Five Dollars

Cromemco

64KZ

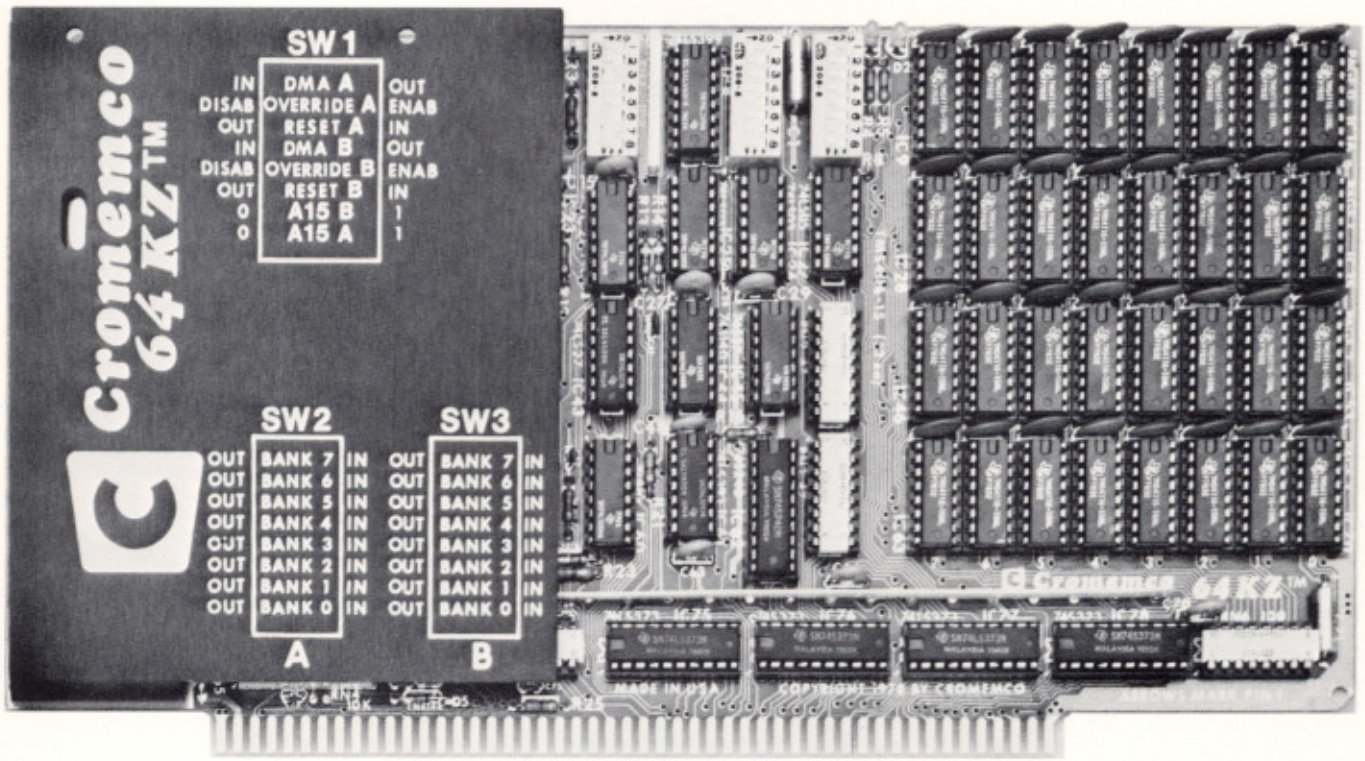
Random Access Memory

Instruction Manual

Cromemco

64KZ

Random Access Memory



Cromemco™
incorporated
Tomorrow's Computers Today
280 BERNARDO AVE. MOUNTAIN VIEW, CA 94043

Part No. 023 - 0008

January 1980

Table of Contents

LIST OF ILLUSTRATIONS

LIST OF TABLES

Section 1
Introduction

Introduction

The Cromemco 64KZ is an S-1ØØ bus compatible 65,536 byte (64 Kbyte) read/write memory board. The 64KZ incorporates the TMS 4116-15 16K X 1 bit dynamic RAM chip to achieve its high memory density while maintaining a true 25Ø nsec (max) access time. This means the 64KZ reliably operates in 4 MHz Z8Ø systems with absolutely no wait states. The Cromemco 64KZ memory board offers the following outstanding and versatile features:

- 64 Kbytes of read/write memory on one S-1ØØ memory board.
- A true access time of 25Ø nanoseconds (maximum).
- Z8Ø and 8Ø8Ø CPU compatibility.
- Organization as two independent 32 Kbyte memory blocks — BLOCK A and BLOCK B.
- BANK SELECT allowing memory expansion beyond 64 Kbytes.
- Powerful DMA configuration options with DMA OVERRIDE.
- Automatic 64KZ enable or disable after a system RESET.
- All significant BLOCK A and BLOCK B options independently switch selectable.

Technical Specifications

MEMORY CAPACITY:	65,536 BYTES (64 KBYTES)
MEMORY TYPE:	TMS 4116-15, 16 X 1 DYNAMIC RAM (or equivalent)
MEMORY ACCESS TIME:	25Ø NANOSECONDS (MAXIMUM)
WAIT STATES @ 2 MHZ:	NONE REQUIRED
WAIT STATES @ 4 MHZ:	NONE REQUIRED
BUS COMPATIBILITY:	S-1ØØ
POWER REQUIREMENTS:	+ 8 VOLTS @ 1.8 AMPERES (MAXIMUM) +18 VOLTS @ .45 AMPERES (MAXIMUM) - 18 VOLTS @ .Ø3 AMPERES (MAXIMUM)
OPERATING ENVIRONMENT:	Ø - 55 DEGREES CELSIUS

Section 2
Operating Instructions

Operating Instructions

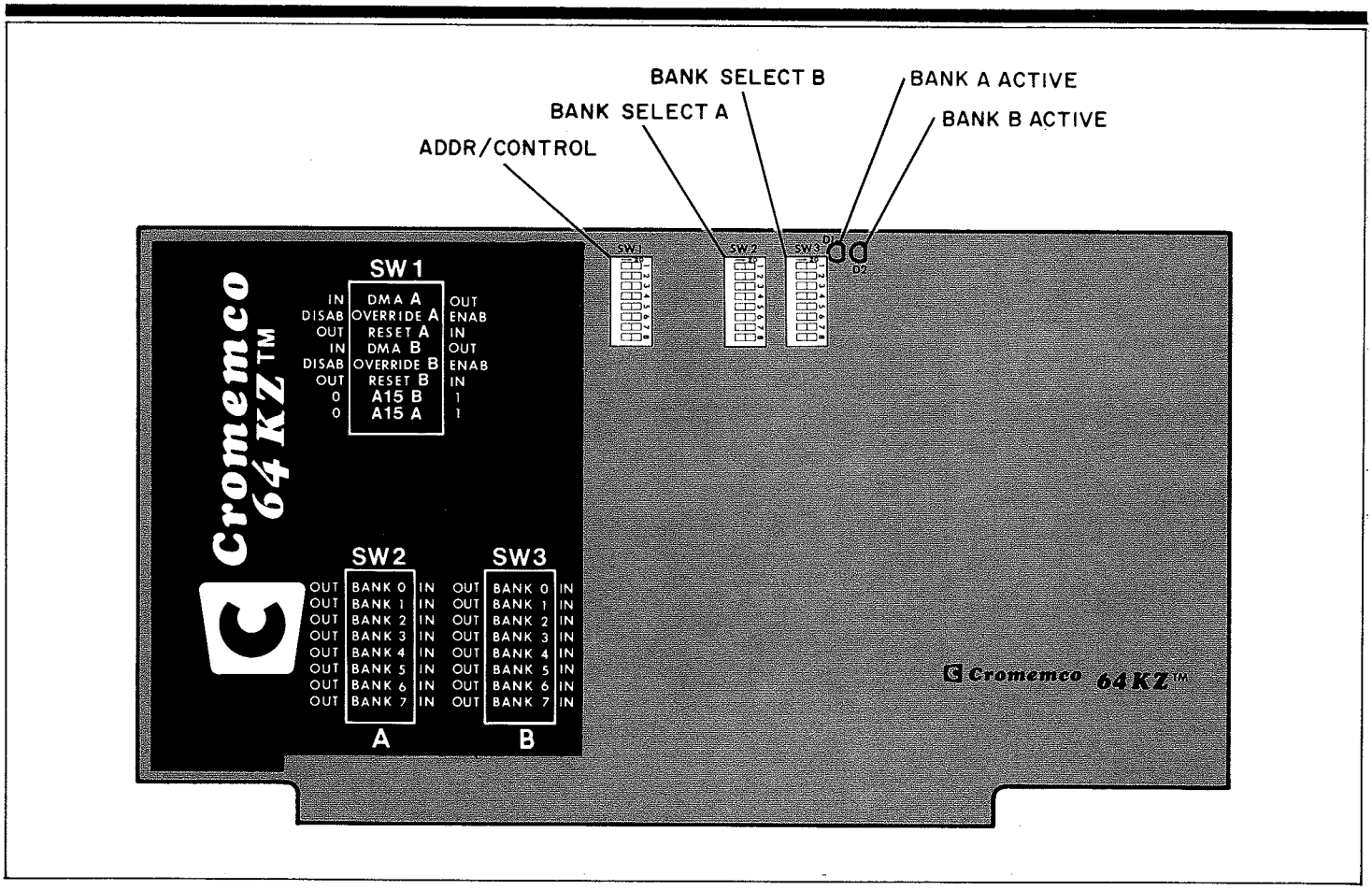
The OPERATING INSTRUCTIONS provide all information necessary to operate the 64KZ board in your Z80 or 8080 S - 100 bus system. The instructions begin with a 64KZ operational overview and summary of switch selectable options. The remainder of the instructions discuss each switch selectable 64KZ option from a system point of view. Careful reading of Section 2 should enable you to tailor-fit the 64KZ to your specific system requirements.

2.1 Switch Options - An Overview

Before plugging the 64KZ into an empty S-100 bus slot, the board should be configured by setting three 64KZ switch groups. This section provides a brief description of each switch function, followed by three example configurations which typify the spectrum of 64KZ applications: a "stripped down" no options configuration; a 64KZ which shadows a ROM bootstrap loader program; and a 64KZ used in a Direct Memory Access DAZZLER® system.

The 64KZ board is functionally organized as two independent 32 Kbyte memory modules, referred to as "BLOCK A" and "BLOCK B". BLOCK A and BLOCK B are configured by setting three switch groups located along the top edge of the board (see Figure 1). Quick reference switch legend artwork appears on the 64KZ

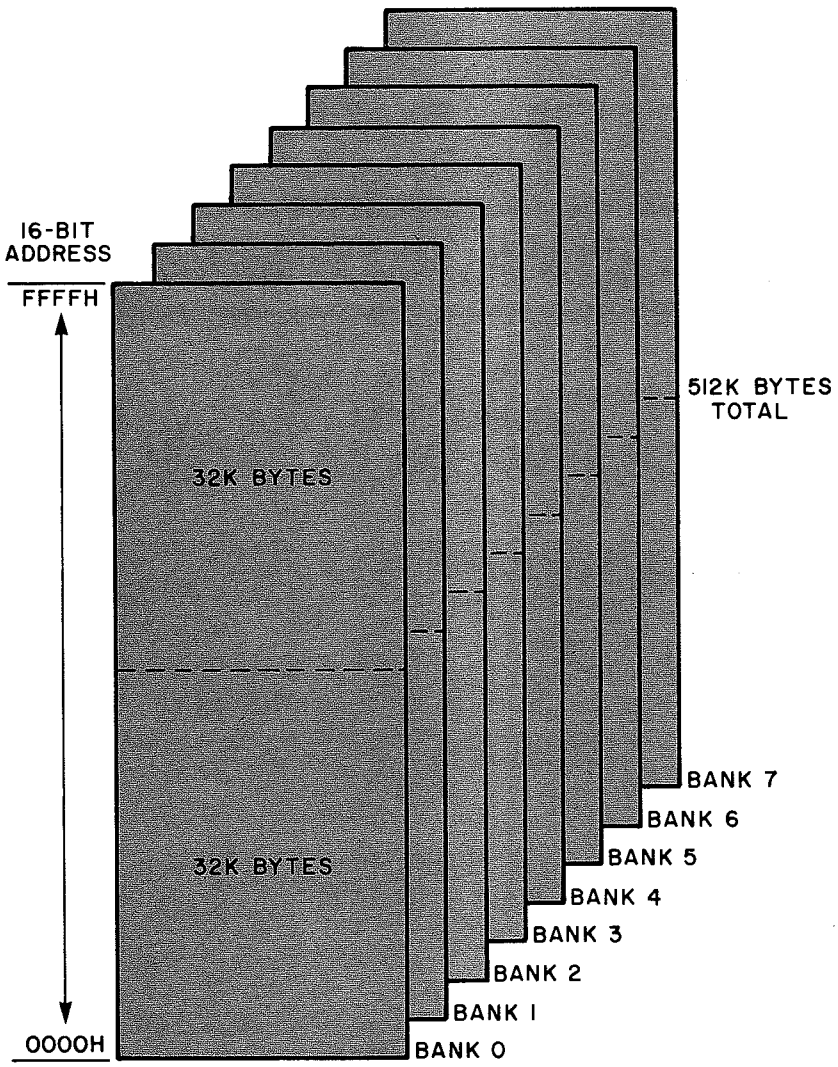
Figure 1 64KZ Switch Locations



heatsink assembly which summarizes each switch function. Those switch functions suffixed by the letter "A" pertain to memory BLOCK A; those suffixed with "B" to BLOCK B.

Memory is further organized into eight 64 Kbyte memory BANKS (BANK Ø - BANK 7), allowing memory expansion up to 8 X 64 Kbytes = 512 Kbytes (see Figure 2). BLOCK A and BLOCK B are independently switch assigned to any combination of memory BANKs with the two BANK SELECT switch groups, and memory BANKs are toggle activated/deactivated under software control. Note that any switch in the three switch groups may safely be re-positioned while power is applied to the 64KZ board.

Figure 2 64KZ Memory Banks



In the SW1 ADDR/CONTROL group, there are four switch functions which control BLOCK A/B: DMA IN/OUT; OVERRIDE ENABLE/DISABLE; RESET IN/OUT and A15 Ø/1 (see Figure 3).

- **THE A15 SWITCHES**

The A15 = Ø maps BLOCK A/B into the lower half of the CPU's 64K direct addressing range (ØØØØ - 7FFFH).

A15 = 1 maps BLOCK A/B into the upper half of the CPU's 64K direct addressing range (8ØØØH - FFFFH).

- **THE RESET SWITCHES**

Setting RESET = OUT unconditionally disables BLOCK A/B after a system RESET or Power-On Clear (P.O.C.), regardless of the BLOCK's current BANK active/inactive status.

Setting RESET = IN unconditionally enables BLOCK A/B after a system RESET or P.O.C., regardless of the BLOCK's current BANK active/inactive status.

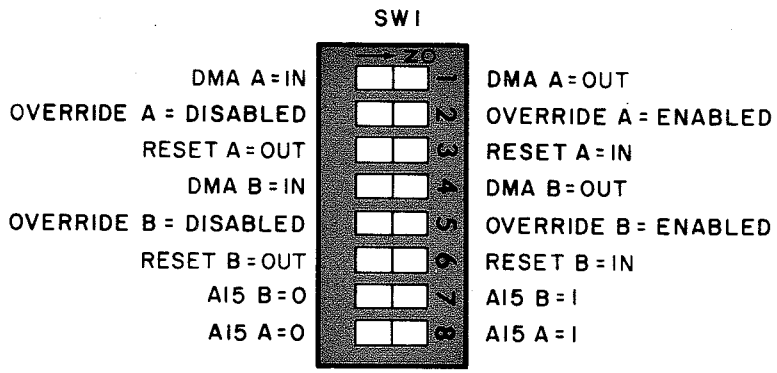
- **THE OVERRIDE AND DMA SWITCHES**

The OVERRIDE and DMA switches control the 64KZ's Direct Memory Access response. Both of these switch settings are irrelevant for non-DMA transfers. In this case, BLOCK A/B is always accessible for read/write access when properly addressed (the correct 16-bit address **and** the correct memory BANK address).

During DMA cycles, setting OVERRIDE = DISABLED again makes BLOCK A/B always available for read/write access when properly addressed (the correct 16-bit address *and* the correct memory BANK address). This mode may correctly be thought of as normal direct addressing (no DMA vectoring), and since OVERRIDE = DISABLED, switch setting DMA IN/OUT is irrelevant.

Setting OVERRIDE = ENABLED effectively collapses all memory BANK boundaries during DMA (memory BANK boundaries are OVERRIDDEN), and board enabling or disabling is contingent upon whether DMA = IN or DMA = OUT. In this case, BLOCK A/B

Figure 3 Addr/Control Switches



enables for DMA read/write access when 16-bit addressed if DMA = IN; and BLOCK A/B automatically disables when DMA = OUT, thereby allowing DMA vectoring to memory with DMA = IN.

- **THE BANK SELECT SWITCHES AND INDICATORS**

Switch groups SW2 and SW3 assign BLOCKS A and B to any combination of memory BANKs (none, one, several or all). Switch group SW2 controls BLOCK A and SW3 controls BLOCK B (see Figure 4).

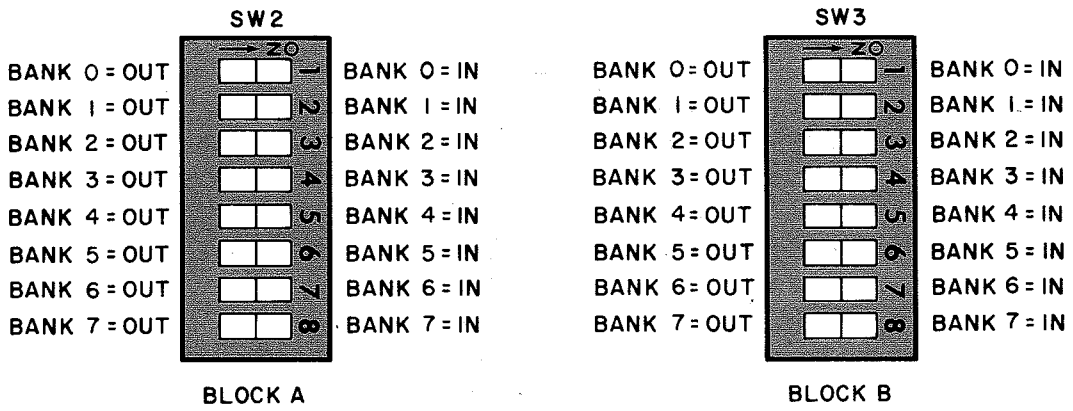
Setting BANK N = OUT logically removes BLOCK A/B from memory BANK N. When BLOCK A/B goes inactive in response to a BANK SELECT control word output by the CPU, the corresponding green BANK ACTIVE indicator light extinguishes (D1 indicates BLOCK A activity, D2 indicates BLOCK B activity).

Setting BANK N = IN logically places BLOCK A/B in memory BANK N. When BLOCK A/B goes active in response to a BANK SELECT control word output by the CPU, the corresponding BANK ACTIVE indicator lights.

EXAMPLE 1

This example illustrates how one might configure the 64KZ card in a "no options" mode which assumes no multiple memory BANKs and no automatic DMA vectoring. With the switch settings shown in Figure 5, the 64KZ is always "in" the memory map spanning the entire 64 Kbyte address space. The board automatically enables after a RESET or a P.O.C. since RESET A = RESET B = IN; the board remains in the memory map for all non-zero software generated BANK SELECT control words since BANK Ø - BANK 7 = IN for both BLOCK A and BLOCK B; and the board is always available for DMA read/write access since OVERRIDE A = OVERRIDE B = DISABLED (DMA IN/OUT is then irrelevant).

Figure 4 64KZ Bank Select Switches



The EXAMPLE 1 configuration assumes the 64KZ constitutes the entire system memory. In such a case, any software operating system must be loaded into RAM memory by manually toggling in, then executing a bootstrap program via system front panel switches. The next example configuration assumes a system containing a ROM resident bootstrap loader program which is shadowed by (shares overlapping address space with) the 64KZ.

EXAMPLE 2

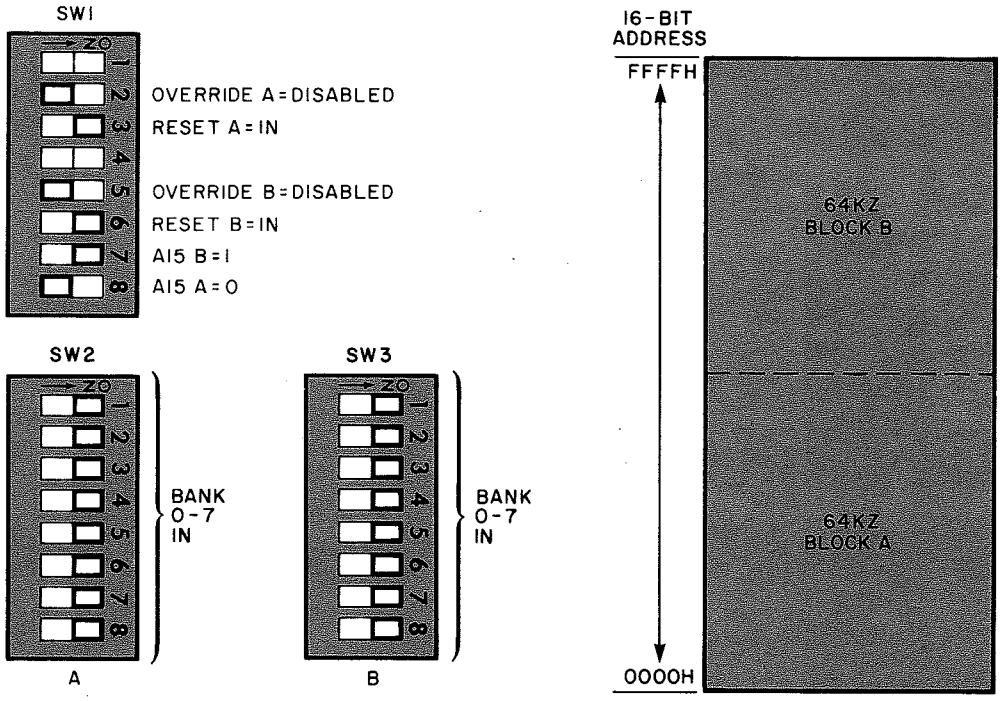
This example illustrates how one might configure the 64KZ card for use in a Cromemco Disc Operating System (CDOS). With a 64KZ card in the system, CDOS would typically be configured with program CDOSGEN to use all available 64 Kbytes of read/write memory. The CDOS program is transferred ("booted") from magnetic diskette to read/write memory for execution by RDOS, a program spanning addresses CØØØH - C3FFH and resident in ROM memory on the Cromemco 4FDC Floppy Disc Controller card.

The sequence of events for a CDOS boot are:

(1) RDOS reads a loader program for the first diskette sector into read/write memory area ØØ8ØH - Ø1ØØH.
(2) A jump to ØØ8ØH is then executed.
(3) The loader program at ØØ8ØH - Ø1ØØH first enables memory BANK Ø only, then completes the transfer of CDOS from diskette to roughly the uppermost 12-15 Kbytes of read/write memory.

Switch settings on the 4FDC card allow the user options of completely disabling or enabling RDOS; of removing or retaining RDOS in the memory map after a CDOS boot; and of "coming up" in RDOS after several console RETURN keystrokes and booting CDOS only when the direct command "B" (Boot) is issued, or automatically executing the RDOS boot

Figure 5 Example 1 No Options 64KZ Switch Settings



routine in response to several console RETURN key strokes.

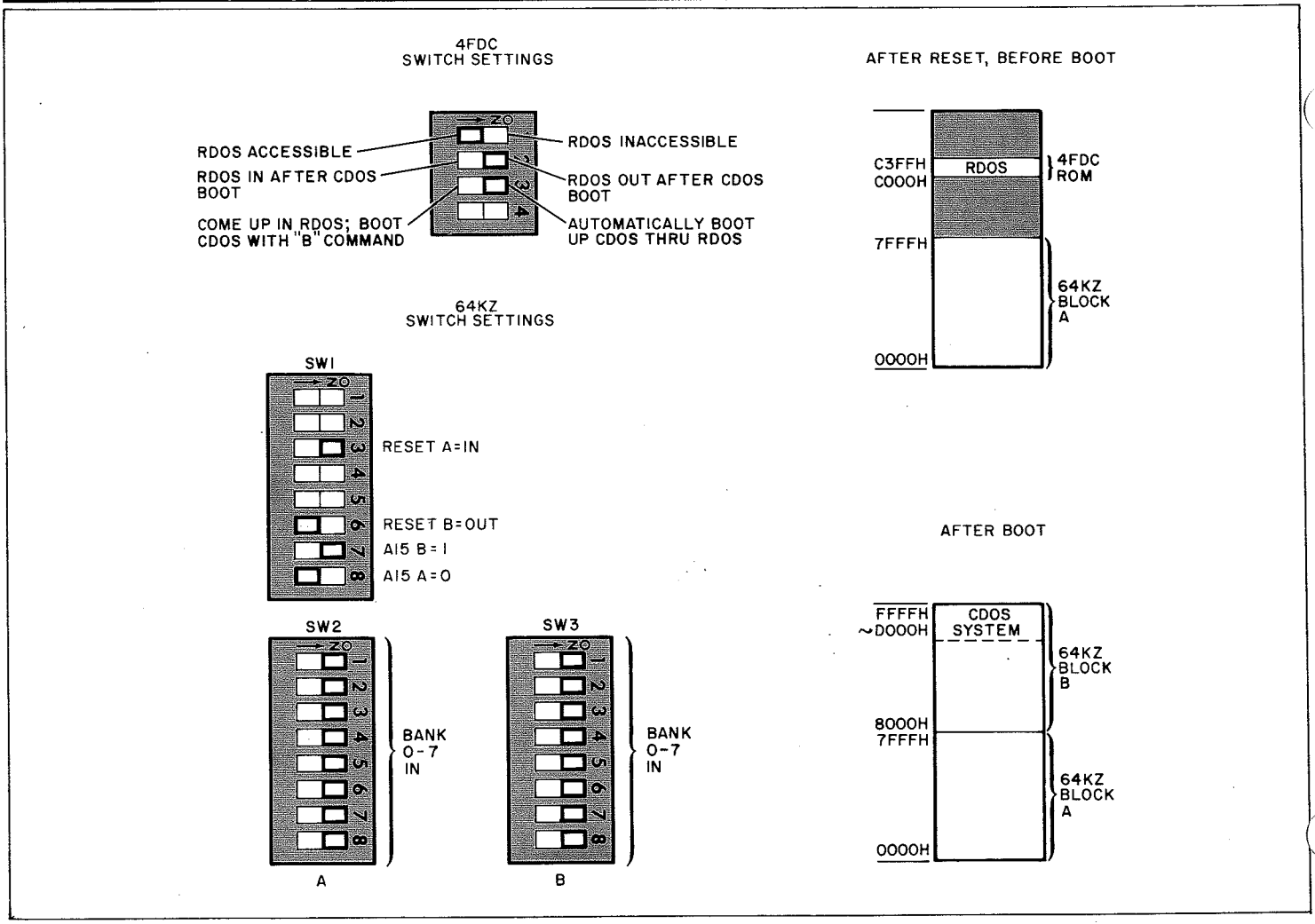
Assuming the 4FDC and 64KZ switch settings shown in Figure 6, CDOS automatically boots up after each system RESET or P.O.C. when the console RETURN key is depressed several times. The rationale behind the switch settings follows. First, BLOCK B, which is assigned to the upper 32K of memory, must disable after a RESET or P.O.C. to avoid a conflict with the shadowed RDOS ROM program located at CØØØH - C3FFH. This is accomplished by setting 64KZ switch RESET B = OUT. 4FDC switch number 2 must be positioned ON so as to disable RDOS after boot (RDOS is disabled at the same time memory BANK Ø is enabled). 4FDC switch number 3 is positioned ON to automatically start the RDOS boot routine after several RETURN key strokes, and finally 64KZ switch BLOCK B, BANK Ø = IN so as to activate the upper 32 Kbytes of read/write memory as RDOS is disabled. The resulting memory map after CDOS has been loaded into 64KZ memory is shown in Figure 6.

The next example illustrates use of the 64KZ DMA OVERRIDE feature in conjunction with a Cromemco DAZZLER® color television interface.

EXAMPLE 3

Assume in addition to the CDOS boot option discussed in EXAMPLE 2, you desire to operate the 64KZ in a CDOS system which contains a Cromemco DAZZLER® graphics board set. The DAZZLER® provides a general purpose interface between your computer and a color TV receiver. The DAZZLER® uses high-speed Direct Memory Access (DMA) to read

Figure 6 Example 2 Boot CDOS Configuration



the "picture memory area" of the host computer, and translate the information into a color TV signal (for further details, reference Cromemco's DAZZLER® Instruction Manual, *part number Ø23 - ØØØ3).*

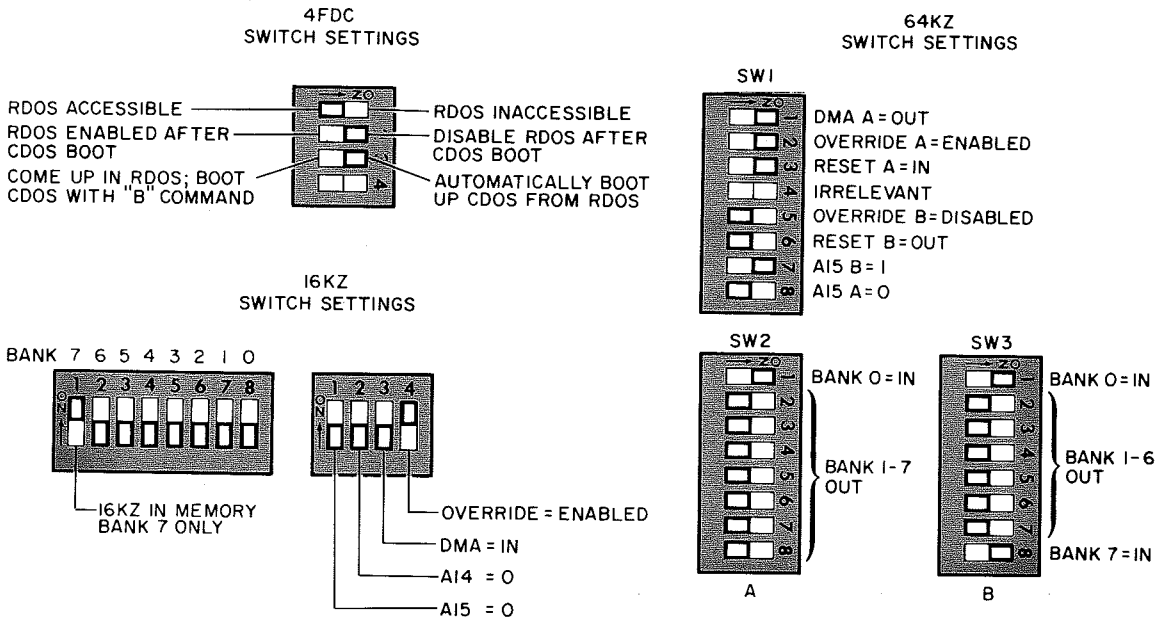
The DAZZLER® can display either a 512 byte picture, or a X4 resolution 2 Kbyte picture. For the purpose of this example, assume you choose to use a Cromemco 16KZ read/write memory board to store the TV picture, a program located in BLOCK A of a 64KZ to do the picture processing, and a program in BLOCK B of the same 64KZ to handle all I/O transfers between the picture processing program and picture memory. The 16KZ board, like the 64KZ, features memory BANK SELECT and DMA OVERRIDE. The 16KZ's memory capacity is 16 Kbytes, allowing eight separate X4 resolution 2 Kbyte pictures to be simultaneously stored on the board (this capacity might be useful in generating animated TV displays where one picture is displayed while the other seven are being processed for subsequent display).

With the 4FDC, 16KZ, and 64KZ switch settings illustrated in Figure 7, there are five active areas in the system memory map (see Figure 8).

RDOS ROM ON THE 4FDC BOARD: This 1 Kbyte memory module automatically boots up CDOS from diskette (loads the CDOS program into roughly the uppermost 15K of memory in BLOCK A, BANK Ø) after a system RESET or a P.O.C. when the RETURN key is pressed several times, and disables after CDOS is loaded.

64KZ RAM BLOCK A: This 32 Kbyte memory module exists in memory BANK Ø only spanning addresses ØØØØH - 7FFFH. The module enables after a system RESET or a P.O.C., and disables during all DMA cycles. Initially, RDOS loads the bootstrap program at starting address ØØ8ØH which then transfers the CDOS system program to the uppermost 15K of memory. Subsequently, BLOCK A would be loaded with a DAZZLER® picture processing program from diskette.

Figure 7 Example 3 Switch Settings



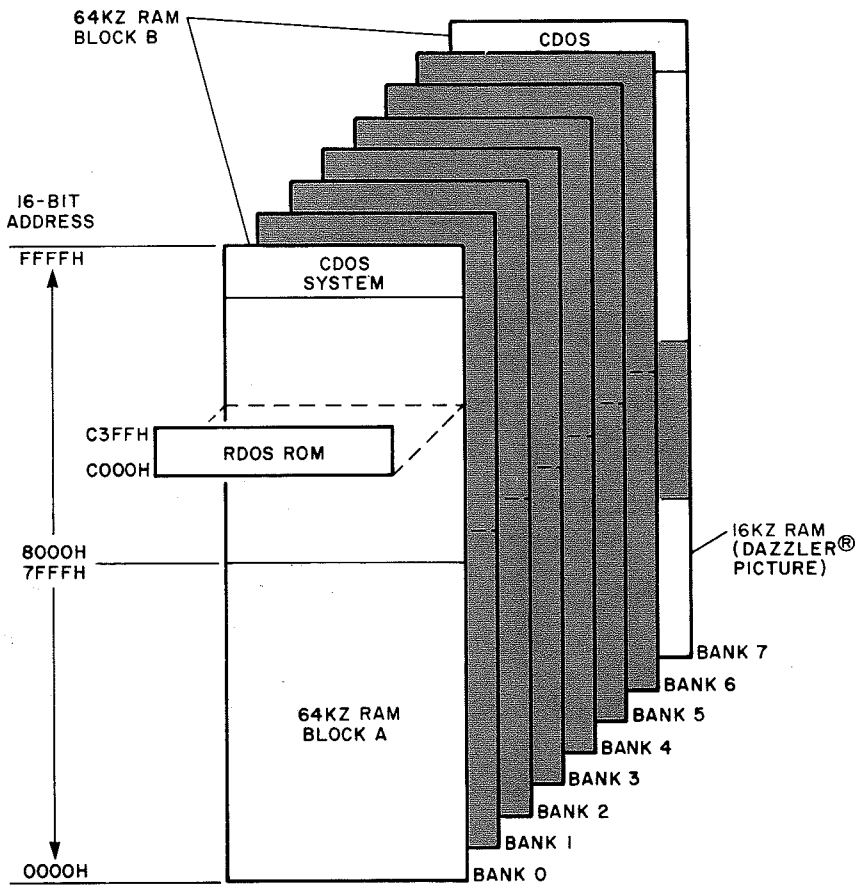
64KZ RAM BLOCK B: This 32 Kbyte memory module exists in memory BANK Ø and BANK 7 spanning addresses 8ØØØH - FFFFH. The module disables after a system RESET or a P.O.C. to avoid a conflict with the shadowed RDOS ROM program. BLOCK B is activated in BANK Ø at the same time that RDOS is disabled, and its uppermost 15K is then loaded with the CDOS system program. Subsequently, BLOCK B would be loaded from diskette with an I/O driver program which links the DAZZLER® picture memory with the picture processing program in BLOCK A. In this example, BLOCK B is available for DMA and non-DMA read/write access in both BANK Ø and BANK 7.

16KZ RAM (DAZZLER® PICTURE): This 16 Kbyte memory module exists in memory BANK 7 only spanning addresses ØØØØH - 3FFFH. The module automatically disables on a system RESET or P.O.C. (memory BANK Ø = OUT controls this function on the 16KZ board). Any DMA read/write operation to an address in the range ØØØØH - 3FFFH automatically vectors to the 16KZ board since OVERRIDE = ENABLED and DMA = IN (and disables 64KZ BLOCK A since DMA = OUT). The 16KZ is also available for non-DMA read/write access when correctly addressed in memory BANK 7.

The overall system operation would then sequence as follows (refer to Figure 9):

(1) The picture processing program in BLOCK A, BANK Ø would generate a read/write request to DAZZLER® picture memory and pass the data and picture address to the I/O driver program in BLOCK B, BANK Ø.

Figure 8 Example 3 Memory Map



(2) *The I/O driver program would then switch memory BANK 7 IN and memory BANK Ø OUT by outputting the appropriate control word to output ports 4ØH on both the 64KZ and the 16KZ boards. This enables BLOCK B and the 16KZ picture memory, and disables BLOCK A. Notice that BLOCK B* must *be in BANK 7 to complete the data transfer; otherwise the CPU will lose contact with the I/O driver program in BLOCK B after the BANK switch.*

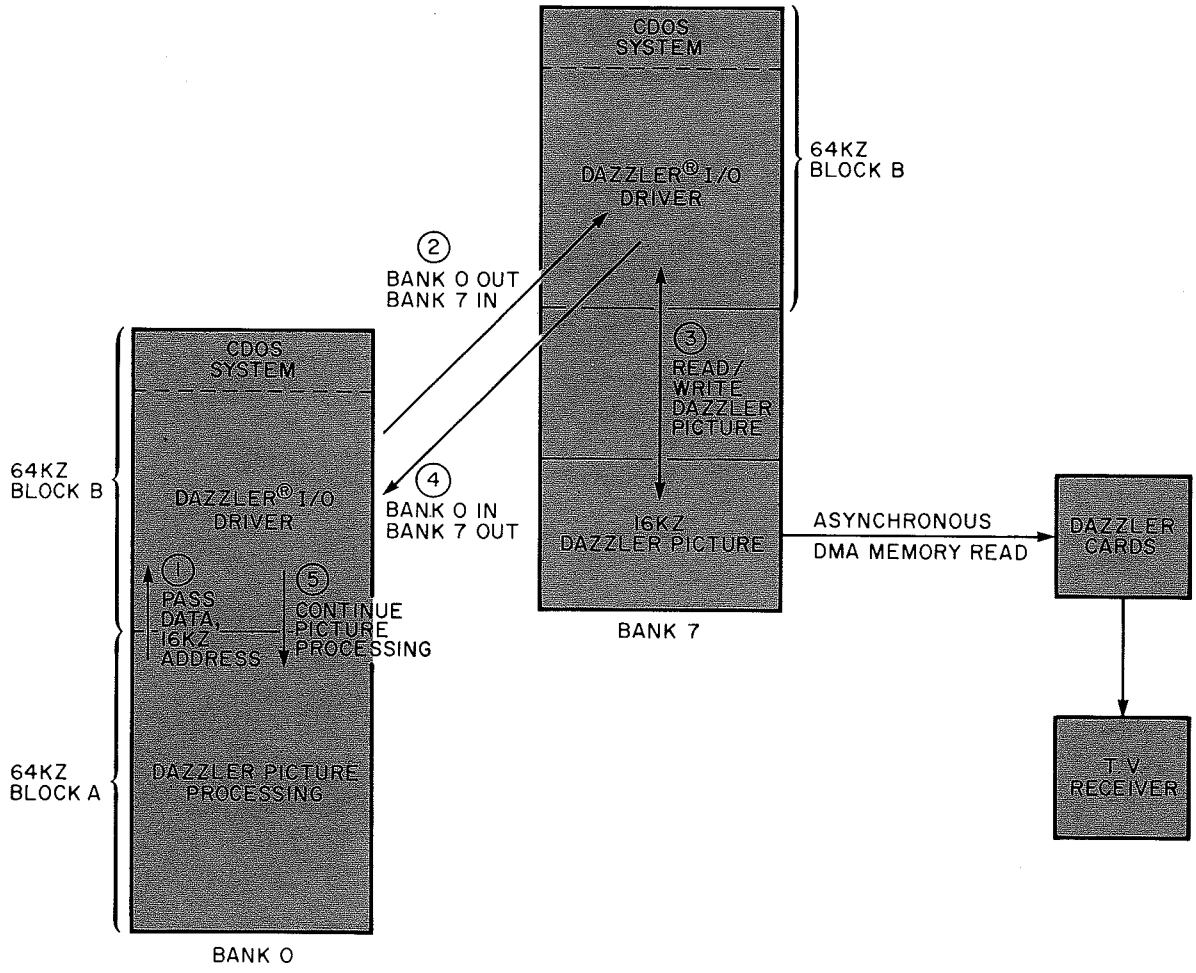
(3) *The I/O driver program then transfers data to or from 16KZ DAZZLER® memory.*

(4) *After the data transfer, BANK Ø is switched back IN and BANK 7 is switched OUT. Notice that the I/O driver program in BLOCK B, BANKs Ø and 7 provides program continuity between BANKs Ø and 7 since BLOCK B is mapped into both BANKs.*

(5) *The I/O driver program then passes control back to BLOCK A for further picture processing.*

(6) *Asynchronously with all of the above sequential events, the DAZZLER® interface cards periodically request and receive Direct Memory Access to the 16KZ memory board. All CPU processing is suspended until each DMA transfer is completed. During each DMA, the 16KZ board unconditionally enables for DAZZLER® memory read cycles, and BLOCK A, BANK Ø unconditionally disables to preclude a data bus conflict. After processing the DMA transfer is completed, the CPU resumes processing from the point of interruption.*

Figure 9 Example 3 DAZZLER® Data Flow



2.2 Addressing The 64KZ

Addressing a byte on the 64KZ for either DMA or non-DMA access involves three levels of selection: choosing a memory BANK, a memory BLOCK and finally choosing a byte in 4116 RAM.

Memory banks are activated and de-activated under software control when the system CPU outputs a BANK SELECT control word to an integral OUT PORT 40H contained on each 64KZ board (see Section 2.3). Memory BLOCK and 4116 RAM selection are decoded from the sixteen bit address A0 - A15 sent out by the CPU on the S-100 bus (see Figure 10).

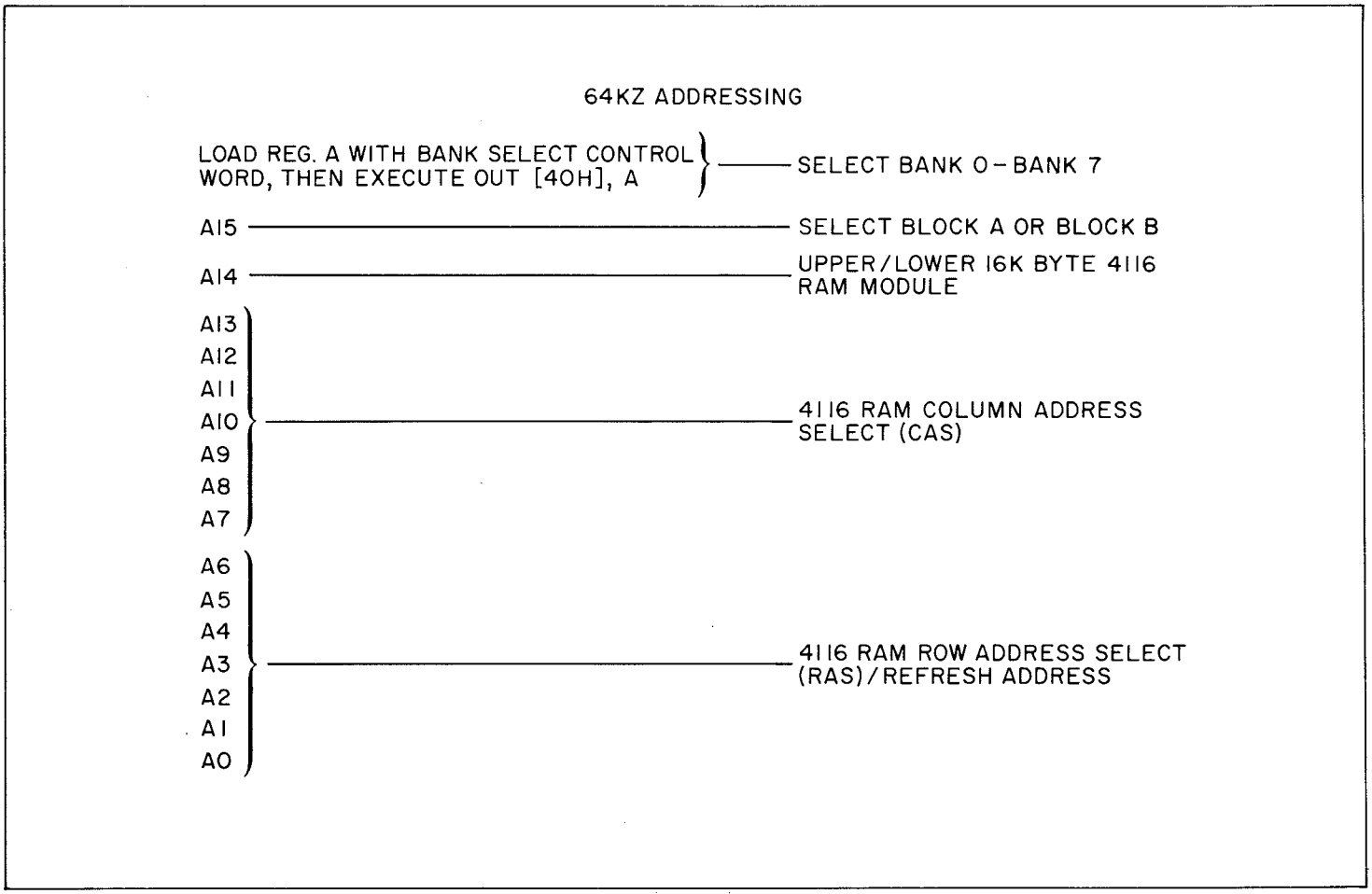
Since memory BLOCK A and B are 32 Kbyte modules, high order address line A15 is hardware compared to BLOCK A/B switch settings in 64KZ switch group SW1 to generate BLOCK SELECT.

The 4116 RAM is a 16K X 1 bit chip with seven multiplexed address pins. Eight parallel addressed 4116s then form a 16 Kbyte module with each chip dedicated to one bit of memory data byte D0 - D7. Two sets of eight-parallel-addressed 4116s then form a 32 Kbyte memory BLOCK, and within the BLOCK, address line A14 is used internally to select the "upper" or "lower" 16 Kbyte module.

One-of-16 Kbits on each 4116 are selected by address lines A0 - A13. Address lines A0 - A6 are applied first to the seven 4116 address lines to generate one-of-128 Row Address Select (RAS), and shortly thereafter address lines A7 - A13 drive the same seven 4116 address lines to generate one-of-128 Column Address Select (CAS).

Since the 4116 is a dynamic memory chip, it must be **refreshed** periodically to maintain data integrity. Refresh is accomplished by addressing each of the 128 row addresses every 2 milliseconds (max) and strobing the 4116 $\overline{RAS}$ input line; or alternately by performing a memory read or write cycle which addresses each of the 128 row addresses at least once every 2 milliseconds.

Figure 10 64KZ Addressing



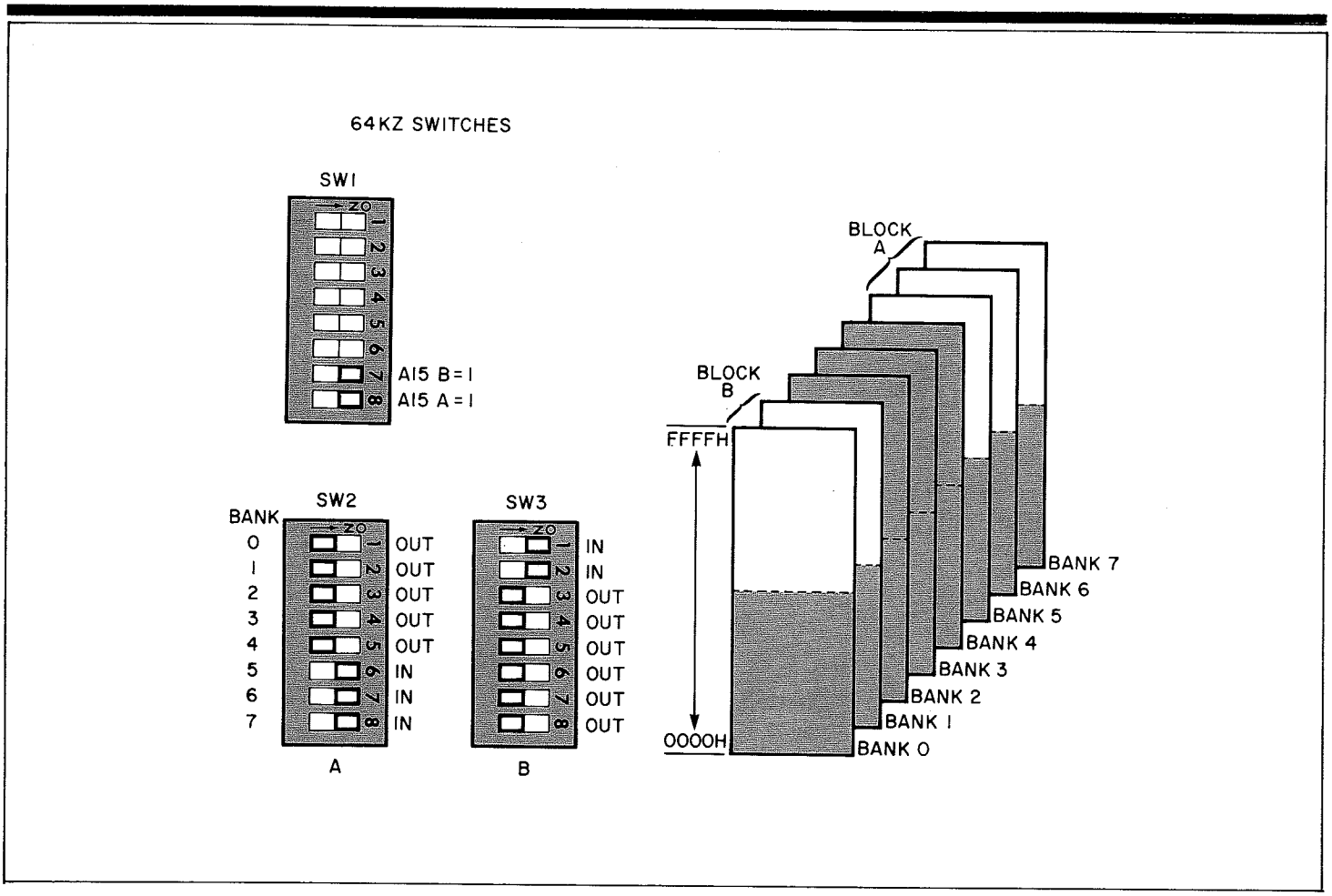
The 64KZ board has been designed with the following division of responsibilities: **the user** switch assigns memory BANKs and memory BLOCKs, and executes software to enable or disable memory BANKs: **the 64KZ hardware** automatically generates BLOCK SELECT, 16 Kbyte module select, RAS and CAS from S-100 bus address lines A0-A15, and also maintains 4116 refresh during all processor cycles except DMA (see Section 2.4). The next section closely examines BLOCK SELECT and BANK SELECT operational considerations.

2.3 Block And Bank Select

As stated above, the 64KZ is logically partitioned into two independent 32 Kbyte memory modules, referred to as BLOCK A and BLOCK B. The BLOCKs may be memory mapped into the upper or lower half of the CPU's 64K direct addressing range with the A15 switches in the SW1 switch group, and may also be placed in any combination of memory BANKs with the BANK SELECT switch groups SW2 and SW3. Cromemco memory boards which also feature BANK SELECT are: the 4KZ RAM card; the 16KZ RAM card; the 8K BYTESAVER II 2708 PROM card; the 16KPR 2708 PROM card; and the 32K BYTESAVER 2716 PROM card. Each of these cards may, in addition to the 64KZ, be memory mapped into a specific 16-bit address area and into any combination of memory BANKs with convenient switch settings, and **all** cards respond to the same software generated BANK SELECT control word output by the system CPU.

Both 64KZ memory BLOCK A and BLOCK B are logically placed in memory BANK N (BANK 0 - BANK 7) by positioning the corresponding switch BANK N = IN; a BLOCK is logically removed from memory BANK N by positioning the corresponding switch BANK N = OUT. A memory BLOCK may be

Figure 11 Example 4 Configuration



placed in any combination of memory BANKs (none, one, several or all). Note that setting BANK Ø - BANK 7 = OUT completely removes BLOCK A/B from the memory map, except possibly after a system RESET or during DMA cycles (see Sections 2.4 and 2.5).

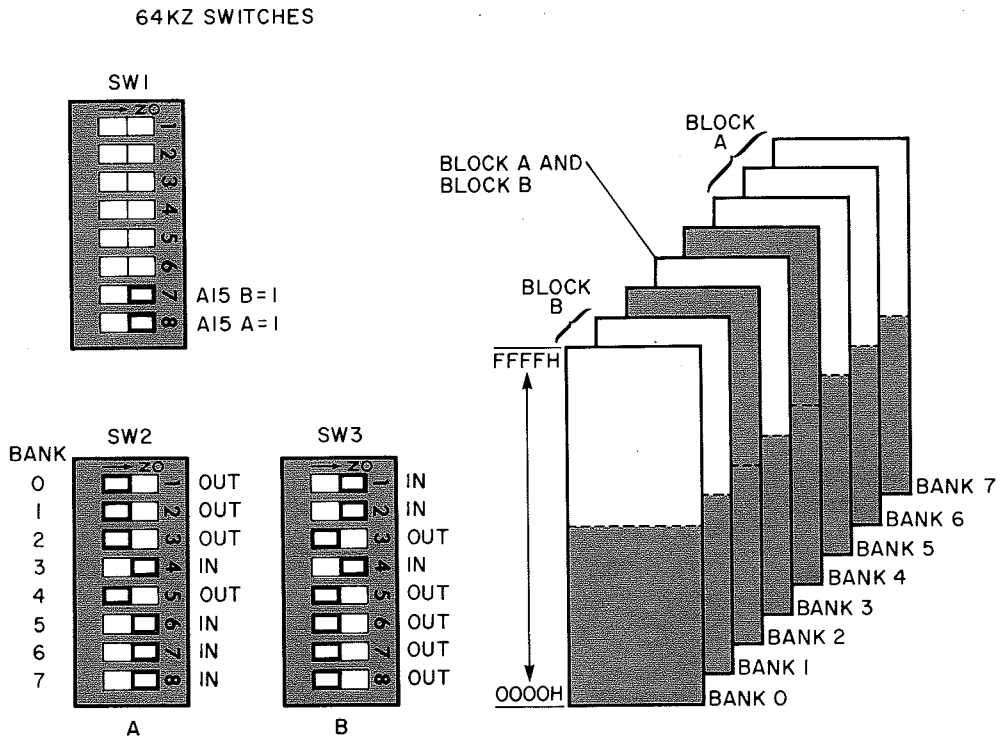
EXAMPLE 4

Setting the 64KZ switches as shown in Figure 11 produces the memory map shown in the same figure. Note that BLOCK A and BLOCK B have both been assigned to the same 16-bit address space (8ØØØH - FFFFH), but in disjoint memory BANKs.

EXAMPLE 5

The 64KZ switch settings shown in Figure 12 produce the memory map shown in the same figure. Notice that BLOCK A and BLOCK B conflict (both may be simultaneously enabled) in memory BANK 3. If memory BANK 3 is activated, a conflict will result when the CPU memory reads a 8ØØØH - FFFFH address, as both BLOCK A and BLOCK B will be actively attempting to drive the S - 1ØØ Data in bus lines DIØ - DI7. While no physical damage to the 64KZ would result, this type of configuration is not recommended as any memory read data from the conflict memory area is unpredictable.

Figure 12 Example 5 Configuration



The two foregoing examples illustrate an important point. The 64KZ, and other Cromemco memory cards with BANK SELECT, may be configured so as to place memory modules in an overlapping 16-bit address space. In such cases, BLOCK A, BLOCK B, and any other system memory module with BANK SELECT, should be placed in **disjoint** memory BANKs to preclude memory read conflicts. While doing this eliminates one conflict source, a software induced conflict may also result as discussed later in EXAMPLE 6.

Memory BANKs are activated and de-activated under software control. Each Cromemco memory card with BANK SELECT contains an integral output port with port address = 40H. The CPU controls memory BANK activity by outputting a **BANK SELECT control** word to all system output ports with address 40H. Each bit of the control word manages one memory BANK. BIT Ø (LSB) controls BANK Ø, BIT 1 controls BANK 1, and so on. Outputting a logic 1 control word bit activates its corresponding memory BANK; outputting a logic Ø control word bit de-activates its memory BANK. Carefully note that if 64KZ BLOCK A/B is in **any** memory BANK activated by the BANK SELECT control word, then the BLOCK enables for both DMA and read/write access, and the green BANK ACTIVE indicator D1 for BLOCK A (D2 for BLOCK B) lights indicating BLOCK A/B is available for read/write access. If BLOCK A/B is in **no** memory BANK activated by the BANK SELECT control word, then the BLOCK disables (floats) thereby clearing the way for some other enabled memory module to occupy the vacated 16-bit address space. When BLOCK A/B is switched into an inactive memory BANK, its green BANK ACTIVE indicator extinguishes.

EXAMPLE 6

Assume your system contains both a Cromemco 64KZ and 16KZ memory card. Also assume the boards are configured as shown in Figure 13.

Then:

- *Executing the two instructions below activates memory BANK 3 and BANK 5, and de-activates all others. Since BLOCK B is in BANK 3 and neither BLOCK A nor the 16KZ are in BANKs 3 or 6, then BLOCK A is inaccessible (floating) when the CPU addresses ØØØØH - 7FFFH, and BLOCK B enables when the CPU addresses 8ØØØH - FFFFH for either DMA or non-DMA access since the 16KZ is in an inactive BANK.*

ADDR	OBJECT	MNEMONIC	COMMENT
CØØØ	3E28	LD A,ØØ1Ø1ØØØB	;ØØ1Ø 1ØØØØ INTO REG. A
CØØ2	D34Ø	OUT [4ØH],A	;CONTROL WORD TO OUT 4ØH
CØØ4	– –	– –	;NEXT INSTRUCTION

- *Executing the two instructions below activates memoryBANK 3 and BANK 6, and de-activates all others. Since the 16KZ is in BANK 6 and 64KZ BLOCK B is in BANK 3, both boards are enabled whenever the CPU addresses CØØØH - FFFFH. Notice that even though the 16KZ and BLOCK B are switch mapped into disjoint memory BANKs, a* **software induced** *memory read conflict has been created by simultaneously activating two disjoint BANKs. Thus, care must be exercised to avoid enabling two addresses overlapping memory modules in disjoint memory BANKs at the same time. Also note that no conflict exists when the CPU addresses ØØØØH - BFFFH since 64KZ BLOCK A is inaccessible at ØØØØH - 7FFFH, and only 64KZ BLOCK B occupies 8ØØØH - BFFFH.*

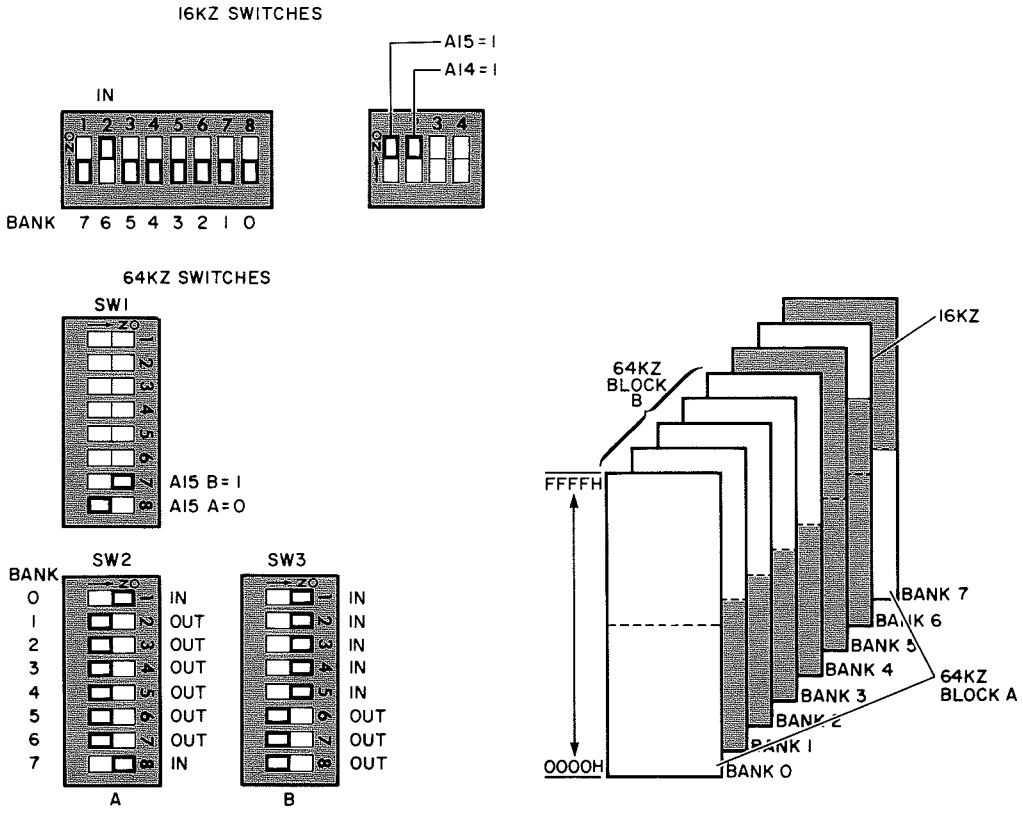
ADDR	OBJECT	MNEMONIC	COMMENT
4ØØØ	3E48	LD A,Ø1ØØ1ØØØB	;Ø1ØØ 1ØØØ INTO REG. A
4ØØ2	D34Ø	OUT [4ØH],A	;CONTROL WORD TO OUT 4ØH
4ØØ4	– –	– –	;NEXT INSTRUCTION

• *Executing the two instructions below activates BANK Ø and de-activates all others. Since both BLOCK A and BLOCK B are in BANK Ø, and the 16KZ is in BANK 7, then both BLOCK A and B are accessible for DMA and read/write access when the CPU addresses ØØØØH - FFFFH, and the 16KZ is inaccessible.*

ADDR	OBJECT	MNEMONIC	COMMENT
ØØØØ	3EØ1	LD A,ØØØØØØØ1B	;ØØØØ ØØØ1 INTO REG. A
ØØØ2	D34Ø	OUT [4ØH],A	;CONTROL WORD TO OUT 4ØH
ØØØ4	– –	– –	;NEXT INSTRUCTION

• *Executing the two instructions on the next page activates BANK 5 and de-activates all others. Since neither BLOCK A nor BLOCK B nor the 16KZ are in BANK 5, then all memory modules become inaccessible after BANK switching. Notice that after these two instructions are executed, the system CPU finds itself with no program code to execute. Therefore, these instructions would not be executed in actual practice.*

Figure 13 Example 6 Configuration



ADDR	OBJECT	MNEMONIC	COMMENT
0000	3E20	LD A,00100000B	;0010 0000 INTO REG. A
0002	D340	OUT [40H],A	;CONTROL WORD TO OUT 40H
0004	--	--	;NEXT INSTRUCTION

As memory BANKs are switched, the user must be careful to maintain **program continuity;** that is, assuring that after BANKs are switched, the CPU correctly fetches the next sequential instruction for execution. Two facts bear directly on maintaining program continuity: first, memory BANKs are activated/de-activated **in unison** during the last machine cycle of the OUT [40H],A instruction; and second, the CPU itself is ignorant of memory BANK boundaries, so it simply proceeds to advance its Program Counter to the next sequential address after the OUT instruction, and fetches opcode for execution. Thus, the last example code segment above which de-activates all BANKs leaves the CPU with no program to execute after BANKs are switched (the CPU would likely read floating data lines as opcode 0FFH, and execute an RST 38H instruction as a result).

A straightforward method for maintaining program continuity is to make one read/write memory module common to all activated memory BANKs, thereby allowing the stack and data to be passed freely among switched memory BANKs. EXAMPLE 3 discussed earlier, and the example below illustrates this idea.

EXAMPLE 7

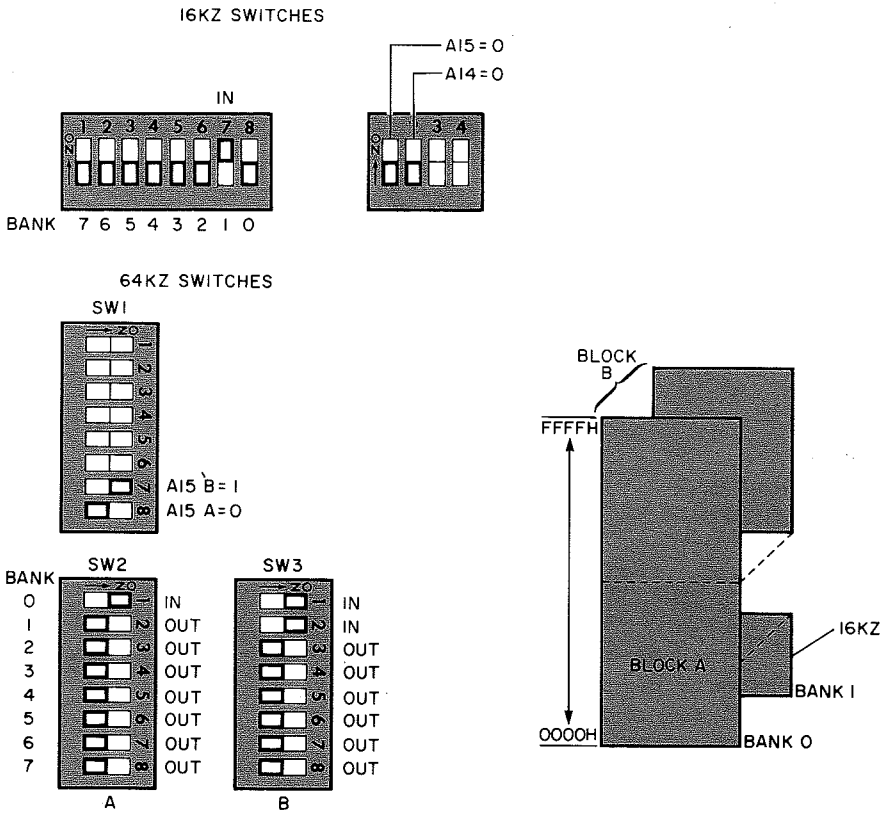
Assume your system contains both a Cromemco 64KZ and a 16KZ configured as shown in Figure 14. Assume also that the contents of 16KZ memory location 1000H, BANK 1, is needed by a program executing in 64KZ memory, BLOCK A, BANK 0. Since the addresses of 64KZ BLOCK A and the 16KZ overlap, the safe way to transfer the data is thru an I/O handler routine in 64KZ BLOCK B (notice that BLOCK A cannot de-activate BANK 0 and activate BANK 1 since contact with the running program would be lost). Sample code to effect the transfer is illustrated below. Initially assume that only BANK 0 is active.

ADDR	OBJECT	LABEL	MNEMONIC	COMMENT
		;		
		; BLOCK A MAIN PROGRAM		
		;		
0400	210010		LD HL,1000H	;LOAD HL WITH 16KZ ADDR
0403	CD00C0		CALL RD16KZ	;CALL 16KZ READ ROUTINE
0406	--	CONT:	--	;READ DATA IN REG. B
		;		
		; BLOCK B 16KZ I/O ROUTINE		
		;		
C000	3E02	RD16KZ:	LD A,2	;ACTIVATE BANK 1 CNTL WORD
C002	D340		OUT [40H],A	;NOW IN BANK 1 WITH 16KZ
C004	46		LD B,[HL]	;16KZ (1000H) TO REG. B
C005	3D		DEC A	;ACTIVATE BANK 0 CNTL WORD
C006	D340		OUT [40H],A	;NOW IN BANK 0 WITH BLOCK A
C008	C9		RET	;RETURN TO 'CONT' IN BLOCK A

Outport port 40H manages eight memory BANKs on all Cromemco memory cards with BANK SELECT. Provisions have been made on the 64KZ to optionally reassign the BANK SELECT port address to a value other than 40H. Each new BANK SELECT port address would then manage eight additional memory BANKs, and these additional BANKs could be used either to expand the gross amount of addressable memory (sixteen 64KZ cards would provide 1.024 Mbytes of RAM organized in sixteen memory BANKs, and still leave room for five other cards in a twenty-one slot S-100 motherboard), or to create more address overlapping memory partitions in multi-user type applications.

The BANK SELECT port address is changed from its factory wired 40H value by cutting five IC60 solder traces (see Figure 15), and installing a 7490S ROM in the empty IC60 socket ("7490S" is a Cromemco assigned part number for a programmed 74S288 32-byte bipolar PROM). With the PROM inserted, the 64KZ hardware still responds to port address 40H = 0100 0000B, but the 74S288 converts the desired port address into 40H data. More specifically, S-100 bus address lines A7, A3, A2, A1 and A0 drive the 74S288 as inputs, and S-100 bus lines A6, A5, A4 bypass the PROM (see Figure 15). Five of the eight 74S288 data out lines then serve as encoded address lines A7', A3', A2', A1' and A0'. The BANK SELECT outport port is then addressed when the combined coded and uncoded lines form address 40H, or when A7' A6 A5 A4 A3' A2' A1' A0' = 0100 0000B. The 74S288 should then be programmed so as to output all zeros when the desired port address drives the five PROM address lines, and to output at least one logic 1 bit on every undesired port address. This scheme results in thirty-two permissible BANK SELECT port addresses; 40H - 4FH and C0H - CFH. Also note that the 74S288 may be programmed to supply 40H data in response to more than one port address.

Figure 14 Example 7 Configuration



The 74S288 PROMs are shipped from the factory with lows in all locations. Highs are irreversibly programmed into selected data bits by blowing Ti-W fuses on the device (see manufacturer's specifications for detailed programming instructions). The 64KZ user may wish to do PROM programming, or optionally the user may order a 74Ø5 part from Cromemco, Inc. When placing a 74Ø5 order, please be sure to specify a BANK SELECT port address(es) in the range 4ØH - 4FH or CØH - CFH, and refer to the ROM by its Cromemco part number, Ø1Ø-Ø116.

2.4 Direct Memory Access

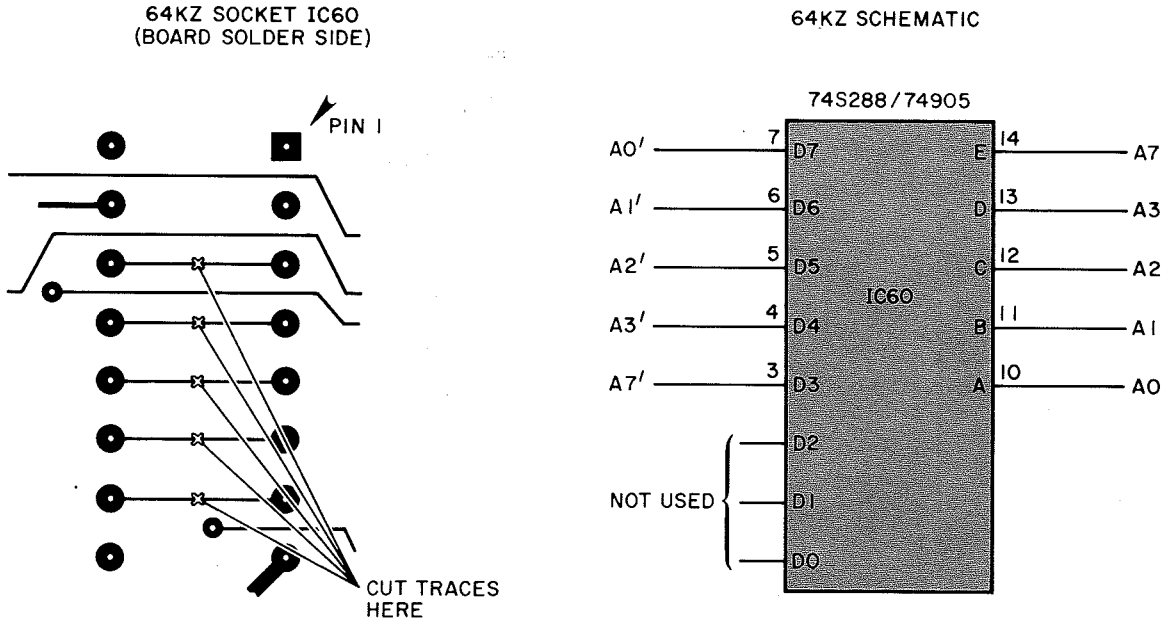
An S-1ØØ bus resident device may gain direct access to system memory without CPU intervention by driving control line $\overline{\text{pHOLD}}$ active low. The CPU acknowledges the DMA request by asserting line pHLDA high, and the DMA device then uses this level as a signal to actively take control of S-1ØØ address, data out and control lines. Control is passed to the DMA device when it asserts S-1ØØ bus lines $\overline{\text{ADDR DSBL}}$, $\overline{\text{DO DSBL}}$, $\overline{\text{C/C DSBL}}$ and $\overline{\text{STAT DSBL}}$ active low, thereby disconnecting the CPU from system memory. At this point the DMA device must seize control of the system address, control and data lines to transfer data to or from memory. DMA implementations are commonly used where a fast, asynchronous memory access, characterized by a high data transfer rate, is required.

Two 64KZ aspects deserve special attention in DMA implementations:

1) In addition to being correctly 16-bit addressed with lines AØ - A15, the 64KZ must also be correctly **BANK addressed.**
2) The 64KZ card does not provide 4116 RAM refresh during DMA.

DMA memory BANK addressing difficulties have been minimized by the 64KZ DMA OVERRIDE fea-

Figure 15 Changing The Bank Select Port Address



ture. With switch OVERRIDE A/B = ENABLED, the 64KZ entirely disregards memory BANKs during the time line pHLDA is active high (DMA memory BANK boundaries are OVERRIDDEN, or ignored); BLOCK A/B enabling then becomes only contingent upon address AØ - A15 and whether DMA A/B is IN or OUT. In essence, only two "DMA memory BANKs" exist with OVERRIDE = ENABLED; the active one containing the enabled memory module with DMA = IN, and the inactive one containing all disabled memory modules defined by switches DMA = OUT.

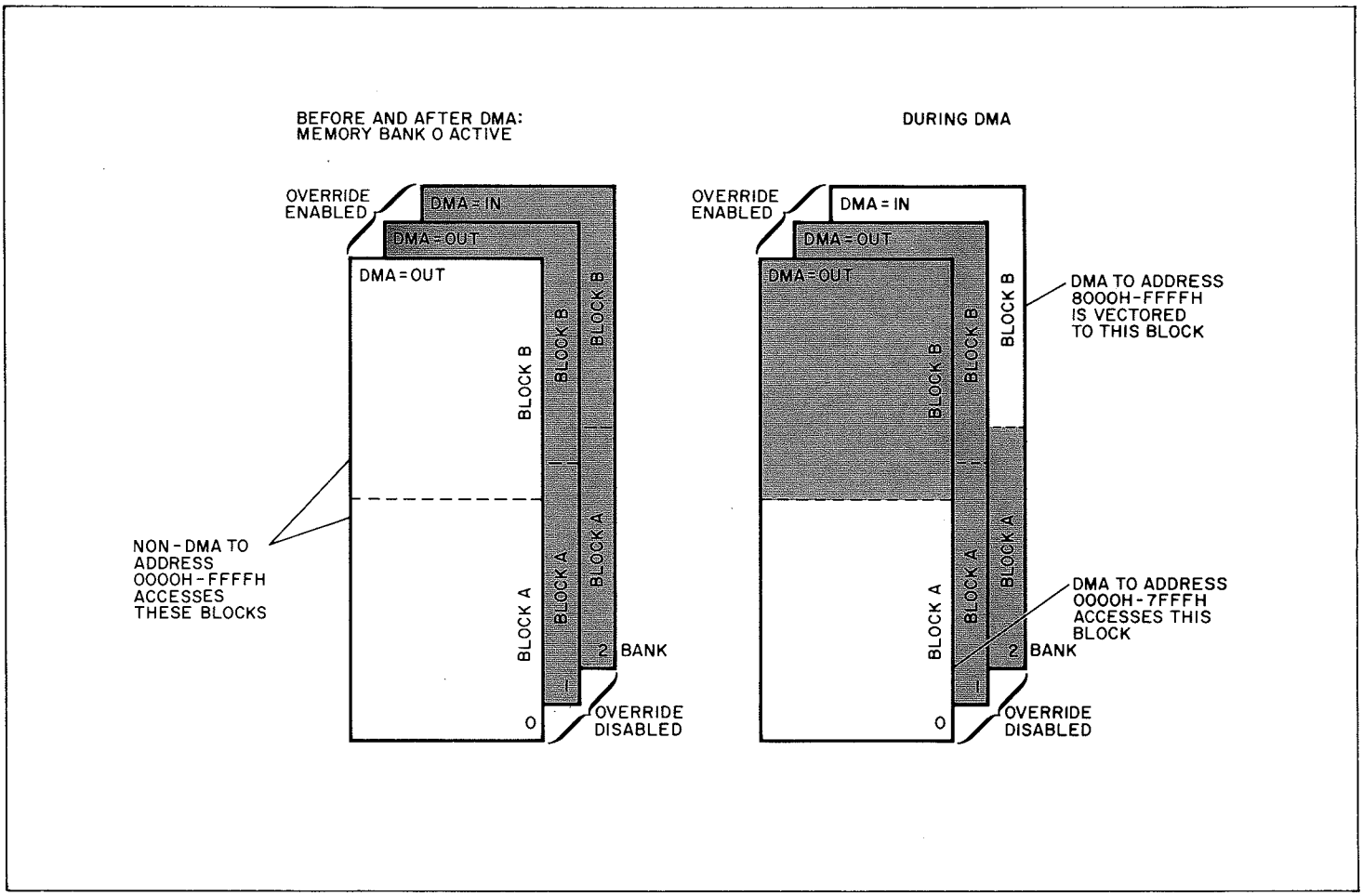
The following example illustrates how to configure the 64KZ in DMA systems with multiple active memory BANKs. The principles and DMA control switch use outlined in the example apply to other Cromemco memory boards with BANK SELECT and DMA OVERRIDE as well. These boards include the 16KZ, the BYTESAVER II, the 32K BYTESAVER and the 16KPR.

EXAMPLE 8

Assume a certain system contains three 64KZ cards. On each card, BLOCK A is assigned to the lower 32K of memory, and BLOCK B to the upper 32K. The first card is assigned to memory BANK Ø, the second to BANK 1 and the third to BANK 2. Assume further that BANK SELECT control word Ø1H is output to all three boards, giving rise to the configuration shown on the left in Figure 16. Then for **non-DMA** *memory read or write cycles, any address in the range ØØØØH - FFFFH accesses the first 64KZ card in BANK Ø.*

For DMA (Figure 16, right), assume all BLOCKs A have OVERRIDE = DISABLED. Then DMA to an address in the range ØØØØH - 7FFFH accesses BLOCK A in BANK Ø since BANK boundaries are **not** *overridden in the ØØØØH - 7FFFH address range, and BANK Ø is active (no differentiation is made between DMA and*

Figure 16 DMA Override



normal CPU addressing since OVERRIDE = DISABLED).

For DMA, assume all BLOCKs B have OVERRIDE = ENABLED, BANKs Ø and 1 have DMA = OUT, and BANK 2 has DMA = IN. Then any DMA to an address in the 8ØØØH - FFFFH range automatically vectors to BLOCK B in BANK 2 (the BLOCK with DMA = IN). BLOCKs B in BANKs Ø and 1 with DMA = OUT automatically disable (float) permitting DMA vectoring to the BLOCK with DMA = IN, even though BANK Ø was active before DMA.

After the DMA transfer is completed, the system memory configuration reverts back to that shown, on the left in Figure 16, and the system CPU resumes program execution from the point of interruption.

Note that it is also possible to include memory BANK switching as part of the DMA device's addressing responsibilities when OVERRIDE = DISABLED. This would not typically be done, however, as the DMA device would also then be responsible for ascertaining pre-DMA memory BANK status and BANK restoration after the DMA transfer. These additional tasks slow down DMA access and complicate the DMA controller. Excepting extraordinary situations where more than one BANK is accessed during DMA, the OVERRIDE and DMA IN/OUT switches would be used to provide complete DMA memory BANK switching control.

During DMA (while pHLDA is active high), the 64KZ suspends dynamic memory refresh. It is then the responsibility of the DMA device to provide memory refresh, **if necessary.**

During normal (non-DMA) operation, the 64KZ provides transparent M1-cycle refresh. That is, both the Z8Ø and 8Ø8Ø processors require at least four clock cycles during an M1 cycle to fetch and decode instruction opcode from system memory. The normal opcode fetch occurs during the first two clock cycles leaving the last two available for memory refresh. This technique has the advantage of requiring no overhead time for memory refresh since refresh occurs during CPU "dead time" (thus the term "transparent refresh"). The disadvantage of the technique is that other means must be provided to supply refresh when the CPU is not executing program code (no M1-cycles). Such a condition occurs when the CPU is HALTed, while the CPU is in the WAIT state in response to a not READY, and during DMA. The 64KZ does provide refresh in the first two instances (CPU HALTed, CPU WAITing), but not during DMA.

The crucial refresh specification which must be observed during DMA is that no more than 2 milliseconds may elapse between either a read or a write cycle to each row address AØ - A7 if the DMA device is providing refresh. If the 64KZ is to provide refresh during DMA, the CPU must execute at least 128 M1-cycles during every 2 millisecond interval.

There are two broadly defined DMA accessing techniques; "DMA cycle stealing" and "burst DMA". Cycle stealing as the term implies, involves periodically stealing from one to several clock cycles from the CPU for the purpose of DMA. For cycle stealing implementations, the 64KZ would typically provide refresh, and the specification then translates to a ratio of CPU to stolen DMA cycles. This ratio must be such that, for every 2 millisecond time interval, the CPU executes at least 128 M1 fetch cycles. Assuming the longest instruction for both the Z8Ø and the 8Ø8Ø (23 T-cycles), the CPU would then conservatively require 128 X 23 X Ø.25 usec = 736 usec out of any 2 msec = 2ØØØ usec interval (assuming a 4 MHz system clock) to provide refresh, or a 37% duty cycle. Assuming a 2MHz clock, the CPU would then require 74% of all clock cycles to assure memory refresh. This simplified analysis assumes that DMA cycles are uniformly distributed among CPU cycles.

In burst DMA implementations, the DMA device typically accesses memory more infrequently, but each access is for a longer period of time than in cycle stealing implementations. If each DMA burst access is less than 1 msec in duration, and spaced more than 1 msec apart, then the 64KZ card itself will provide adequate dynamic memory refresh. If either the DMA access time is lengthened, or the interval between successive accesses is shortened, then it becomes the responsibility of the DMA device to provide refresh. In such a case, refresh may be easily provided by reading from (or writing to) any 1/2 page (128 bytes) of contiguous 64KZ memory at least once ever 2 msec.

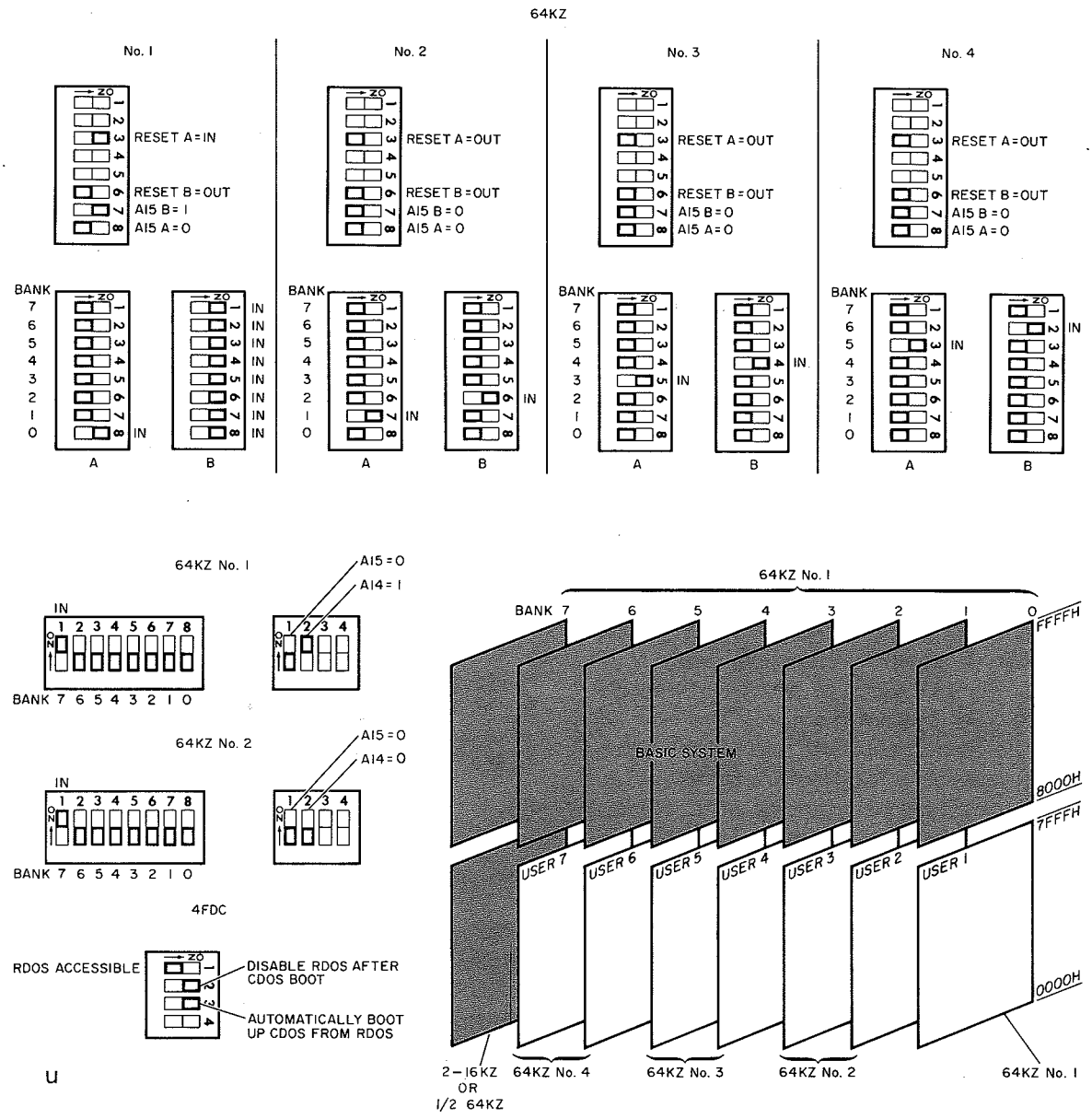
2.5 Multi-User Basic Application

The 64KZ is the ideal memory card for use in a Cromemco Multi-User BASIC system. The Multi-User BASIC system timeshares up to seven different BASIC programs resident in the same S-1ØØ bus system. Each BASIC user is assigned to a different memory BANK (BANKs Ø - 6), and may be allocated either 16 or 32 Kbytes of read/write memory starting at address ØØØØH for program text. The BASIC operating system requires 64 Kbytes of read/write memory. Of the 64 Kbytes, 32 Kbytes spanning 8ØØØH - FFFFH are assigned to all memory BANKs Ø - 7; this area contains the BASIC interpreter program itself and part of the operating system. The remaining 32 Kbytes, spanning ØØØØH - FFFFH, are assigned to memory BANK 7

only. This memory area currently contains most of the system disc and terminal I/O routines.

Figure 17 illustrates how five 64KZ cards or four 64KZ cards and two 16KZ cards may be used to form a fully configured seven user BASIC memory system.

Figure 17 Multi-User Basic



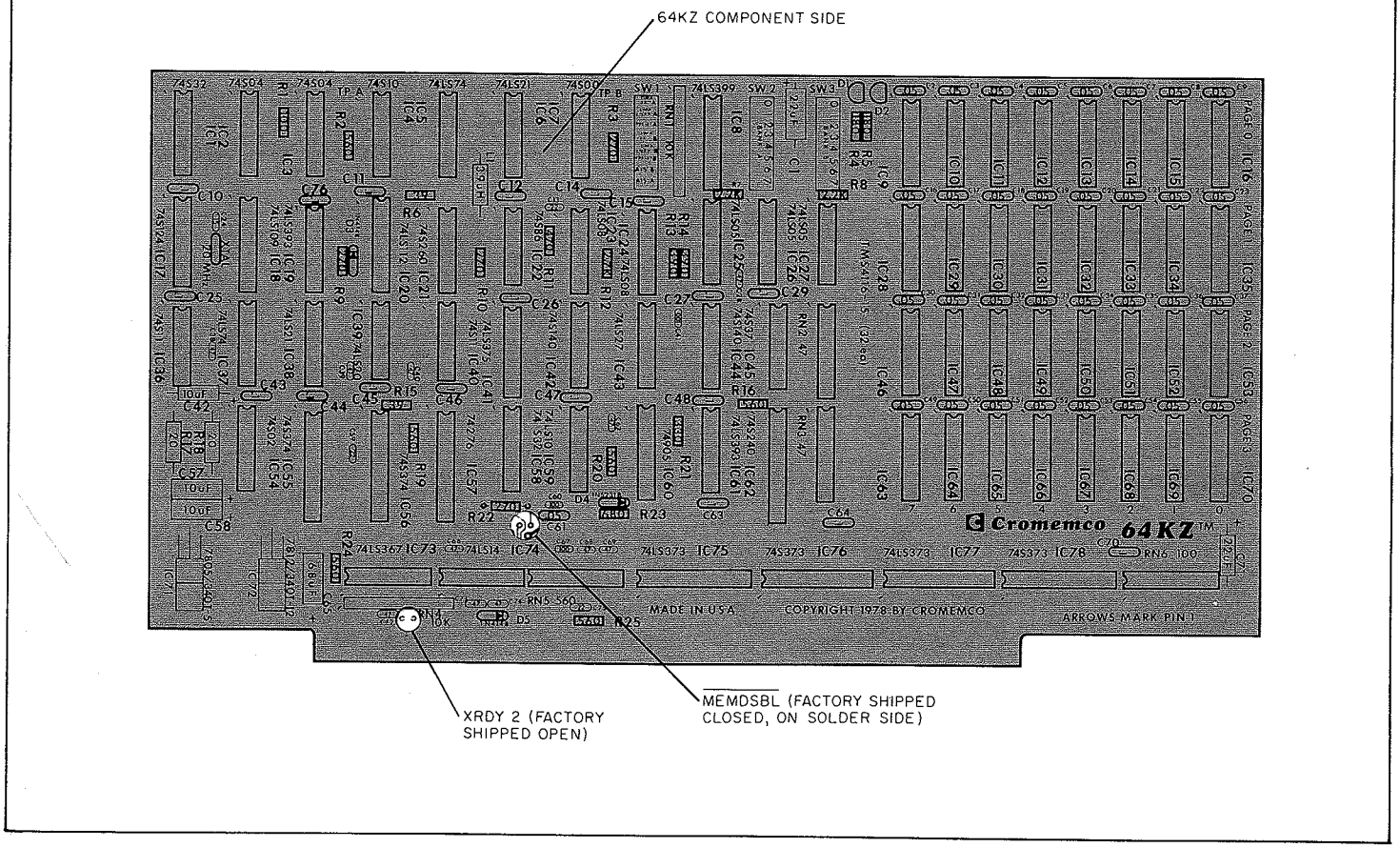
2.6 64KZ Jumper Options

The 64KZ provides two jumper-wire selectable options; MEMDSBL and XRDY 2 (see Figure 18).

MEMDSBL is a function assigned to S-100 bus pin 67 which, when asserted active low, completely disables the 64KZ memory card. This hardware controlled memory disable capability may be removed by cutting the solder trace between the two pads indicated in Figure 18, **on the board solder side.** If your system uses pin 67 for some other function, or if the line is not used at all, Cromemco recommends that you cut the trace. The MEMDSBL function should be left in its factory wired enabled state in systems which require a phantom memory capability.

XRDY2 is a function assigned to S-100 bus pin 12 which, like function pREADY on pin 72 and XRDY 1 on pin 3, indicates that memory is ready to supply read data or to accept write data when the line is active high, or is not ready when pulled low (thereby forcing the CPU to WAIT). If your system uses pin 12 for the XRDY 2 function, a jumper wire should be inserted between the pads located in Figure 18, on the board component side. This allows the 64KZ to monitor the XRDY 2 line for a not ready condition so that it may step in and supply autonomous refresh while the CPU is WAITing (see Section 3). If your system uses pin 12 for some other function, or not at all, leave the jumper pads in their factory shipped open condition (no jumper).

Figure 18 64KZ Jumper Pad Locations



Section 3
Theory of operation

Theory Of Operation

Please refer to the 64KZ Block Diagram shown in Figure 19 and to the 64KZ Schematic Diagram while reading this section.

The 64KZ is functionally built around a 40 MHz local oscillator (IC17 and associated circuitry) and an 8-bit timing shift register (IC55). This relatively high clock frequency allows the 64KZ to periodically latch all important S-100 bus status, control, data and address lines, thereby largely removing 64KZ dependence on CPU timing. The 8-bit shift register provides "25 nsec delayed taps" along the register which are used to generate 4116 dynamic RAM control signals.

Operation begins with the "cycle start detection" logic, which monitors the appropriate S-100 control and status lines, and determines when a memory read or write cycle is being initiated. Flip flops in IC20, two sections of IC57, and one section of IC5 are used to detect the various start conditions. Table 1 summarizes the logic condition which produces a true (logic 1) start condition for each flip flop.

Figure 19 64KZ Block Diagram

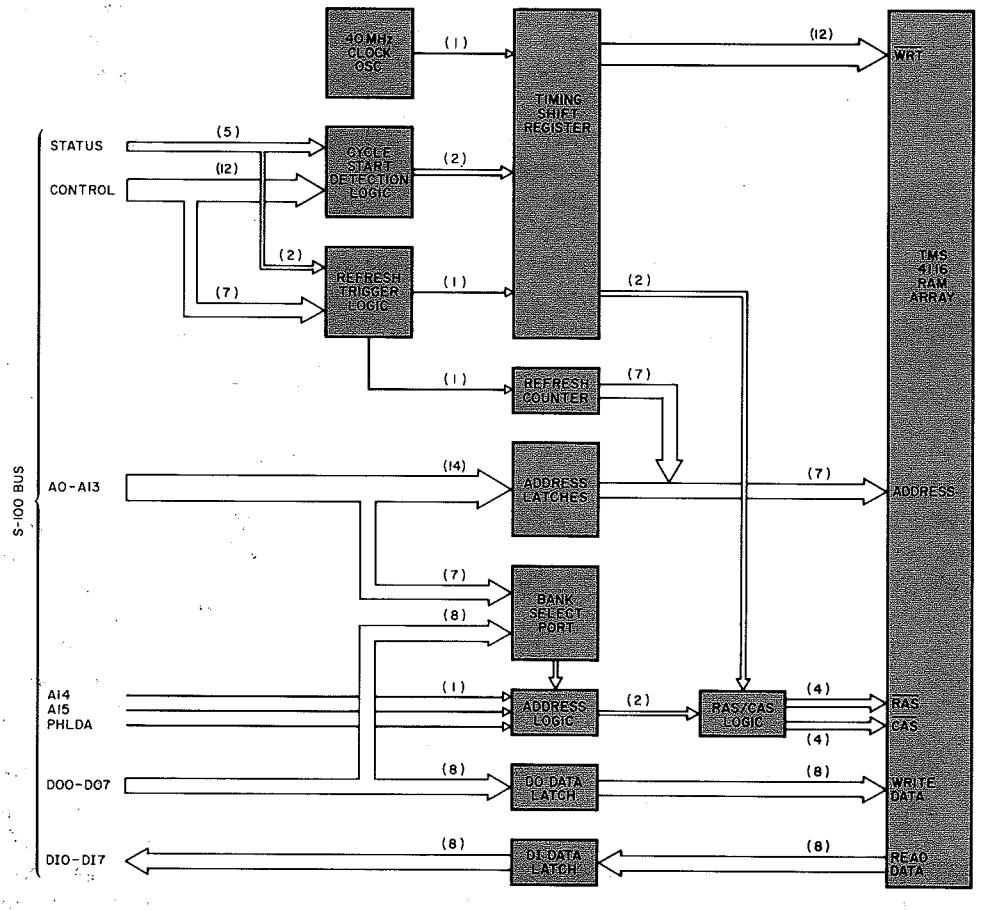


Table 1 Flip Flop Start Conditions

OUTPUT	BOOLEAN EXPRESSION	CYCLE TYPE
IC57 PIN 16	$s\overline{OUT} \cdot sWO \cdot CPU \cdot MREQ \cdot [pSYNC\urcorner\llcorner]$	Z8Ø WRITE
IC2Ø PIN 9	$[CPU \cdot sMEMR \cdot MREQ \cdot \overline{RFSH}]\llcorner\urcorner$	Z8Ø READ
IC2Ø PIN 5	$CPU \cdot pSYNC \cdot [sM1\llcorner\urcorner]$	Z8Ø M1 FETCH
IC57 PIN 15	$sMEMR \cdot pSYNC \cdot \overline{MREQ} \cdot CPU \cdot [Ø2\llcorner\urcorner] +$	8Ø8Ø READ
	$sMEMR \cdot pSYNC \cdot \overline{MREQ} \cdot DMA \cdot [Ø2\urcorner\llcorner]$	DMA READ
IC5 PIN 9	$(CPU+DMA) \cdot \overline{MREQ} \cdot [MWRITE\llcorner\urcorner]$	DMA & F.P.WRITE
	where $CPU = pH\overline{LDA} \cdot \overline{CCDSBL}$ and $DMA = pHLDA \cdot CCDSBL$	

The output of NOR gate IC21 PIN 6 goes low whenever any of the above flip flop outputs go high, and thereby generates a cycle start request signal. The IC5 PIN 9 output start request is first arbitrated against a possible autonomous refresh request. This is necessary since a front panel write can occur at any time while the CPU is HALTed. When the write operation can proceed, IC57 PIN 5 goes high and IC21 PIN 6 goes low. The cycle request signal is then passed to the timing shift register via IC36 PIN 1Ø. The output IC36 PIN 8 goes low whenever a memory cycle occurs for any reason. This signal goes to the address latches IC75 and IC76 to save the current address, and to IC58 PIN 9 to start the shift sequence. Eight sections of IC55 are clocked at 4Ø MHz and arranged as a Johnson Counter, giving a cycle period of 16 clock intervals at 25 nsec each, for a 4ØØ nsec memory cycle. The output of IC5 PIN 8 goes low for 2ØØ nsec, and the recirculated logic pulse from IC55 PIN 9 then forces IC5 PIN 8 high for the following 2ØØ nsec interval. Thus, the basic pulse generated at the various shift register taps is 2ØØ nsec active high, and delayed according to the tap location.

As soon as the cycle request has been detected by the first shift register stage, $\overline{RAS}$ is taken low for all four RAM memory rows. After a 25 nsec allowance for the RAMS to latch AØ - A6, the address multiplexers switch and drive the RAM array with A7 - A13, with the tristate latch output connection performing the actual multiplexing. $\overline{CAS}$ is then taken low on the selected RAM row 5Ø nsec after the address is switched from AØ - A6 to A7 - A13.

The RAM row receiving $\overline{CAS}$ is determined by the combination of A14, A15, address select and BANK SELECT. The RAM array is organized as two independently addressable BLOCKs of 32 Kbytes, with A14 determining which row in the BLOCK is in use. A separate BANK SELECT state flip flop is provided for each BLOCK, together with A15 and DMA control switches. Any combination of the two BLOCKs desired may be accessed, including simultaneous writing. However, attempts at simultaneous reading will not be affected. Finally, a $\overline{MEMDSBL}$ bus line connection is provided for use in systems requiring phantom memory capability.

A 2ØØ nsec wide clear pulse is generated 2ØØ nsec after the start of the shift register sequence which clears all cycle start detect flip flops. This clear pulse resets the controller in readiness for further memory activity. At the same time, IC37 PIN 5 clocks low if the current cycle is a memory write cycle with sM1 true. This condition signifies a front panel write operation, and causes the 64KZ to automatically execute a read cycle after performing the write cycle, thereby allowing the front panel lights to immediately display the newly deposited data.

When $\overline{CAS}$ turns off (goes high), the enable pin of IC78 goes active low causing read data from the RAM array to be latched for S-1ØØ DI bus access. This allows the CPU to use the memory read data at any arbitrary time after the memory cycle is complete. It also permits the front panel lights to show the data present at the currently addressed memory location when execution is stopped, even though the RAM array is busy being refreshed.

Since the 64KZ incorporates the 4116 dynamic RAM chip, provisions must be made to periodically restore the data logic levels in the RAM cells. Two different refresh methods are provided. First, when the 8Ø8Ø or Z8Ø CPU is running, a transparent refresh occurs during states T3 and T4 of an M1 instruction fetch cycle, when needed. IC19 PIN 6 provides a

trigger pulse once every 16 cycles of ϕ2 to request a refresh. IC36 PIN 6 passes on this request to set IC18 PIN 6 at the start of the next M1 cycle. The second half of IC18 is present during the M1 cycle and causes a transparent refresh.

The second method provides autonomous refresh whenever the CPU stops executing M1 fetch cycles (except during DMA). IC3 PIN 6 goes low signifying the occurrence of any system bus state requiring autonomous refresh. IC19 PIN 9 then begins counting ϕ2 clock pulses, issuing a refresh request once every 16 pulses. After arbitration with a possible front panel write pulse in IC58, the refresh request sets IC5 PIN 5 high to request a refresh cycle. Upon completion of the refresh cycle, flip flop IC5 PIN 5 is cleared.

Parts List

Integrated Circuits		Part No.
IC1	74S32	010-0090
IC2-3	74S04	010-0123
IC4	74S10	010-0035
IC5	74LS74	010-0055
IC6	74LS21	010-0060
IC7	74S00	010-0036
IC8	74LS399	010-0115
IC9-16	4116-15*	011-0019
IC17	74S04	010-0123
IC18	74LS109	010-0051
IC19	74LS393	010-0041
IC20	74LS112	010-0126
IC21	74S260	010-0094
IC22	74S86	010-0125
IC23-24	74LS08	010-0064
IC25-27	74LS05	010-0065
IC28-35	4116-15*	011-0019
IC36	74S11	010-0111
IC37	7474	010-0055
IC38	74LS21	010-0060
IC39	74LS20	010-0095
IC40	74S11	010-0111
IC41	74LS175	010-0042
IC42	74S140	010-0138
IC43	74LS27	010-0112
IC44	74S140	010-0138
IC45	74S37	010-0136
IC46-53	4116-15*	011-0019
IC54	74S02	010-0122
IC55-56	74S374	010-0132
IC57	74276	010-0091

Integrated Circuits		Part No.
IC58	74S32	010-0090
IC59	74LS10	010-0063
IC60	74905	010-0166
IC61	74LS393	010-0141
IC62	74S240	010-0139
IC63-70	4116-15*	011-0019
IC71	7805	012-0001
IC72	7812	012-0002
IC73	74LS367	010-0108
IC74	74LS14	010-0061
IC75	74LS244	010-0100
IC76	74S374	010-0132
IC77	74LS374	010-0133
IC78	74S373	010-0085

Capacitors		Part No.
C1	22 UF @ 20V	004-0028
C2-9	.05 UF	004-0027
C10-12	.1 UF	004-0030
C13	22 PF	004-0041
C14-15	.1 UF	004-0030
C16-23	.05 UF	004-0027
C24	18 PF	004-0050
C25-27	.1 UF	004-0030
C28	47 PF	004-0000
C29	.1 UF	004-0030
C30-37	.05 UF	004-0027
C38-40	47 PF	004-0000
C41	.001 UF	004-0043
C42	10 UF @ 20V	004-0032

*Note: Equivalent part numbers are TMS 4116-15NL, MM5290-2, MK8116H, PD416-3, MK4116N-2. These may be substituted for the 4116-15 at Cromemco's option.

Parts List

Capacitors		Part No.
C43-48	.1 UF	004-0030
C49-56	.05 UF	004-0027
C57-58	10 UF @ 20V	004-0032
C59	150 PF	004-0010
C60	100 PF	004-0009
C61	.05 UF	004-0027
C62	47 PF	004-0000
C63-64	.1 UF	004-0030
C65	6.8 UF	004-0034
C66	47 PF	004-0000
C67	100 PF	004-0009
C68-69	47 PF	004-0000
C70	.1 UF	004-0030
C71	22 UF	004-0028
C72-74	47 PF	004-0000
C75-76	22 PF	004-0041
C77	47 PF	004-0022
C78-84	100 PF	004-0009
C85	47 PF	004-0022
C86	22 PF	004-0041

Resistor Networks		Part No.
RN1	10K, 10 PIN	003-0024
RN2-3	47, 16 PIN	003-0022
RN4	10K, 10 PIN	003-0024
RN5	560, 16 PIN	003-0021
RN6	100, 16 PIN	003-0020
RN7	560, 8 PIN	003-0006

Resistors		Part No.
R1	100	001-0007
R2	560	001-0015
R3	270	001-0011
R4-5	180	001-0009
R6	39	001-0002
R7-8	2.2K	001-0021
R9-10	270	001-0011
R11	470	001-0014
R12	2.7K	001-0023
R13-14	390	001-0013

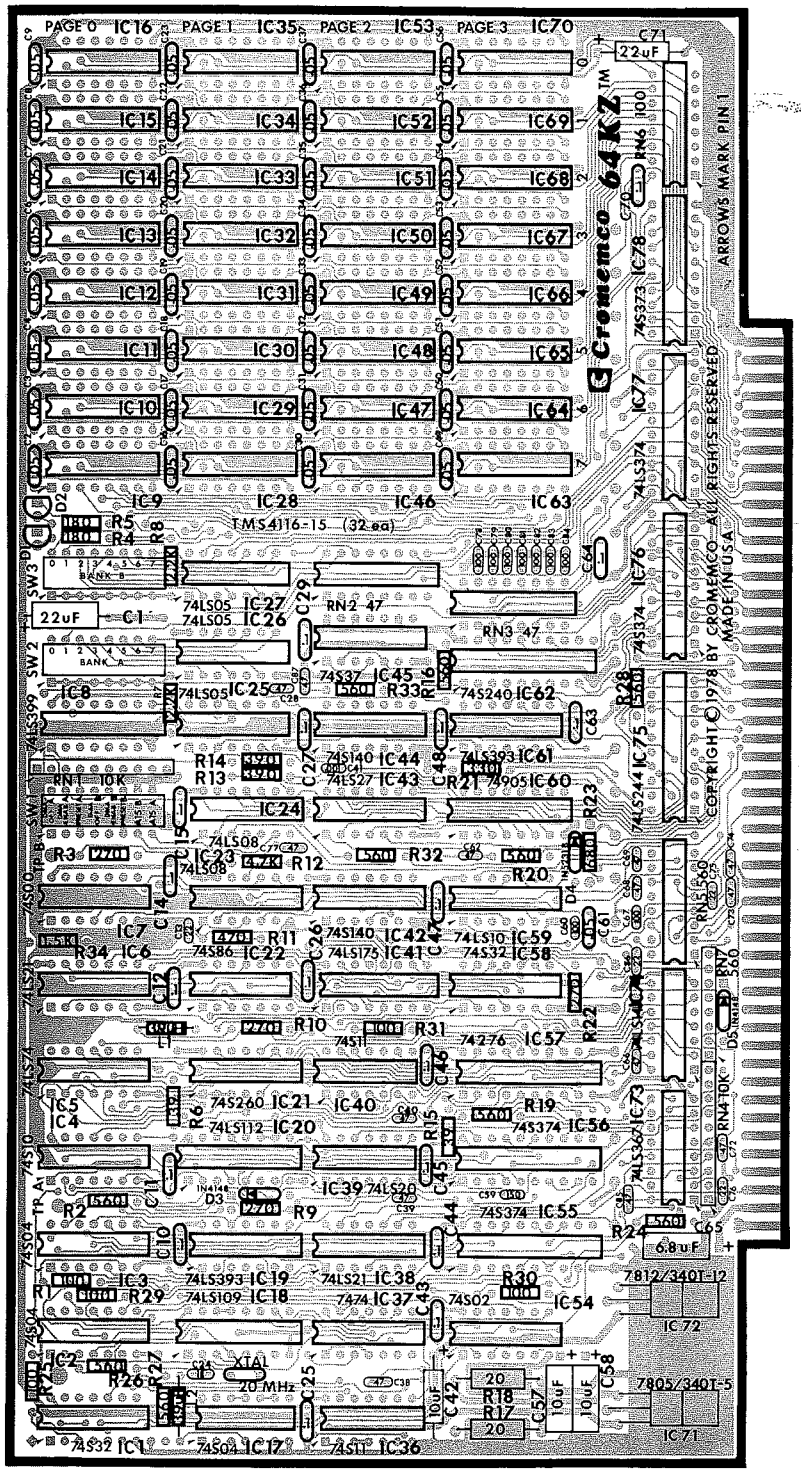
Resistors		Part No.
R15	39	001-0002
R16	560	001-0015
R17-18	20	001-0046
R19-20	560	001-0015
R21	330	001-0012
R22	270	001-0011
R23	680 1/2 W	001-0067
R24	560	001-0015
R25	100	001-0007
R26-28	560	001-0015
R29	100	001-0007
R30	100	001-0007
R31	100	001-0007
R32-33	560	001-0015
R34	1.5K	001-0020

Diodes		Part No.
D1-2	TIL-211 LED	008-0020
D3	1N4148	008-0002
D4	1N5231B, 5.1V	008-0006
D5	1N4148	008-0002

Miscellaneous		Part No.
L1-2	3.9 UH CHOKE	007-0003
XTAL	20 MHZ.	026-0002
3-DIP SWITCH, 8 POS		013-0002
64KZ PC BOARD		020-0014
64KZ BUS BAR		021-0038
64KZ HEAT SINK		016-0059
30-SOCKETS, 14 PIN		017-0001
42-SOCKETS, 16 PIN		017-0002
8-SOCKETS, 20 PIN		017-0004
2-WIRE WRAP POSTS		017-0044
2-THREADED STDOFFS		015-0083
2-STEEL SCREWS		015-0084
2-NYLON SCREWS		015-0085

Documentation	Part No.
64KZ INSTRUCTION MANUAL	023-0008

Parts Location Diagram



Limited Warranty

Cromemco, Inc. warrants this 64KZ memory board against defects in materials and workmanship for a period of Ninety (90) days from the date of delivery to the customer. Cromemco, Inc. will replace or repair at its option their product should it prove to be defective due to defects in materials or workmanship during the warranty period, provided that this product is returned to Cromemco, Inc. postage or shipping prepaid and adequately packaged for shipment to insure against loss. If this product fails after the above Ninety (90) day warranty period, it will be repaired for a fixed prepaid service fee provided that this product is returned to Cromemco, Inc. postage or shipping prepaid and adequately packaged for shipment to insure against loss. Cromemco, Inc. reserves the right to refuse to repair any product that in the discretion of Cromemco, Inc. has been subjected to electrical or mechanical abuse or not handled with reasonable care. The service fee is currently $70 and is subject to change without notice.

Cromemco, Inc. makes no further warranties either expressed or implied with respect to this product and its quality, performance, merchantability, or fitness for any particular use. In no event will Cromemco, Inc. be liable for direct, indirect, incidental or consequential damages. Some states do not allow the exclusion or limitation of implied warranties or liability for incidental or consequential damages, so the above limitation may not apply to some customers.

Cromemco™
incorporated
Tomorrow's Computers Today
280 BERNARDO AVE. MOUNTAIN VIEW, CA 94043

023-0008